LASER XT SERIES

PERSONAL COMPUTER

Technical Reference Manual

For LASER Multi-I/O Card

TABLE OF CONTENT

APPENDIX

CHAPTER 1

INTRODUCTION

1. INTRODUCTION

The Multi-I/O Card is a multifunction enhancement product for the IBM®PC,PC/XT family or compatible computers. This card incorporates Very Large Scale Integration (VLSI) Gate Array technology to reduce PCB area, minimize power consumption and improve reliability.

1.1 FEATURES AND AVAILABLE OPTIONS

The Multi-I/O Card provides standard features including:

- **Floppy disk interface**

  Two double-sided, double-density floppy disk drives are supported.

- **Parallel printer port**

  Interfaces with a Centronics type parallel printer.

- **RS-232C serial interface ports**

  Up to two RS-232C serial interface ports are provided for interfacing with modem, serial printer, remote display terminal or other serial devices.

- **Real - Time Clock**

  With the rechargeable backup battery, the real-time clock allows automatic setting up of time and date every time the computer is turned on.

- **Game Port**

  Connects to game paddle or joystick, for interactive games and graphics software.

- **Diskette Backup (Transcopy) Function**

  Provides diskette duplication of copy-protected or non-copy-protected software. This function is activated via jumper setting and an optional software package. Check with your dealer for details of this software.

The Multi-I/O Card is available in different versions for various levels of system requirements. Some version comes with only one serial interface port. Sockets and connectors are provided to allow upgrading to two serial ports. Refer to the user's manual for details of upgrading to two serial ports.

Another version of this card contains no floppy disk interface. This version is applicable to PC, PC/XT or compatible main units with built-in Floppy Disk Adapter logic.

Newer version (Enhanced) of this card has on board jumpers which allows disabling of some I/O functions when there is conflict with other devices in the system.

1.2 SYSTEM USAGE

The Multi-I/O Card interfaces with a PC, PC/XT or compatible main unit via a 62 pins PCB edge connector (slot). The following I/O Channel lines are used:

A0-A10	Address lines
D0-D7	Data lines
IOR, IOW	I/O Read and I/O Write lines
AEN	Address enable line
TC	Terminal count for DMA operation

RESET DRV	System Reset line
DACK 2	DMA acknowledge for DMA channel 2
DRQ 2	DMA request for DMA channel 2
IRQ2, IRQ3, IRQ4, IRQ5, IRQ6, IRQ7	Interrupt request levels 2,3,4,5,6 and 7
+5V, +12V, -12V	+5V, +12V and -12V DC supply voltages

The following table summarizes the I/O Address, Interrupt Levels and DMA Channels used by each of the functions:

Function	I/O Address (Hex)	Interrupt Level	DMA Channel
Floppy Disk Interface	3F2-3F5	6	2
Parallel Printer Port	378-37A or 3BC-3BE	7	/
RS232C Serial Port (COM1)	3F8-3FF	4	/
RS232C Serial Port (COM2)	2F8-2FF	3	/
Game Port	201	/	/
Real-Time Clock	340-35F or 2C0-2DF	2 or 5	/
Transcopy Function	66F or 6EF or 76F or 7EF	/	2

CHAPTER 2

BOARD LAYOUT, CONNECTORS AND JUMPERS

2. BOARD LAYOUT, CONNECTORS AND JUMPERS

The Multi-I/O Card occupies one 62 pins PCB edge connector (slot) as a typical long card does. However, the two RS232C Serial Interface Ports uses two additional brackets on the back panel of the computer main unit. Therefore, a total of three slots will be required.

2.1 BOARD LAYOUT

The following figure shows the major elements, in particular, the jumper blocks and connectors on the Multi-I/O Card.

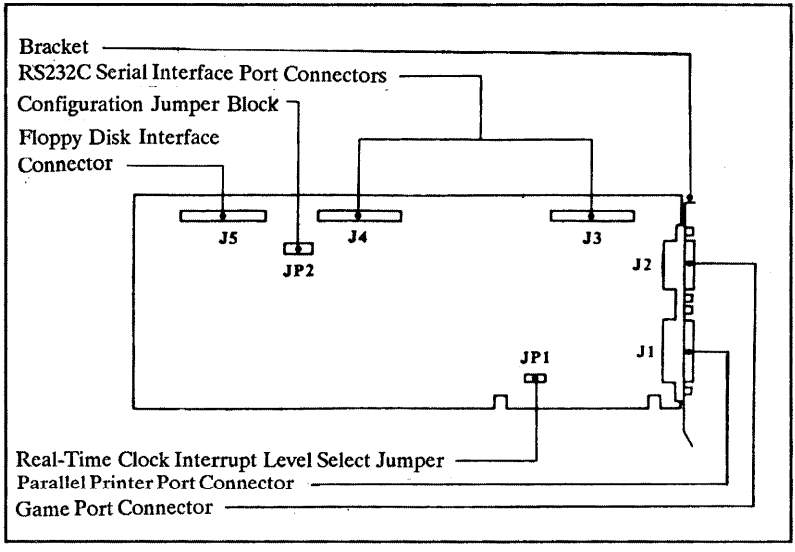


Fig. 2.1 Multi-I/O Board Layout

2.2 CONNECTORS AND JUMPERS

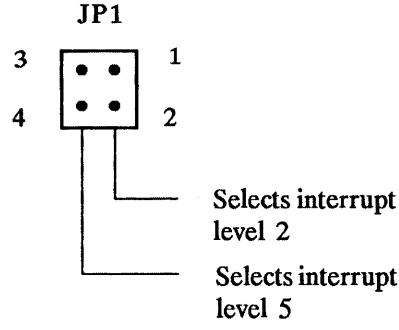
- Connector J1, a 25 pins "D" type female connector, is for connecting to a Centronics standard parallel printer.

- Connector J2, a 15 pins "D" type female connector, is for connecting to a joystick or game paddles.

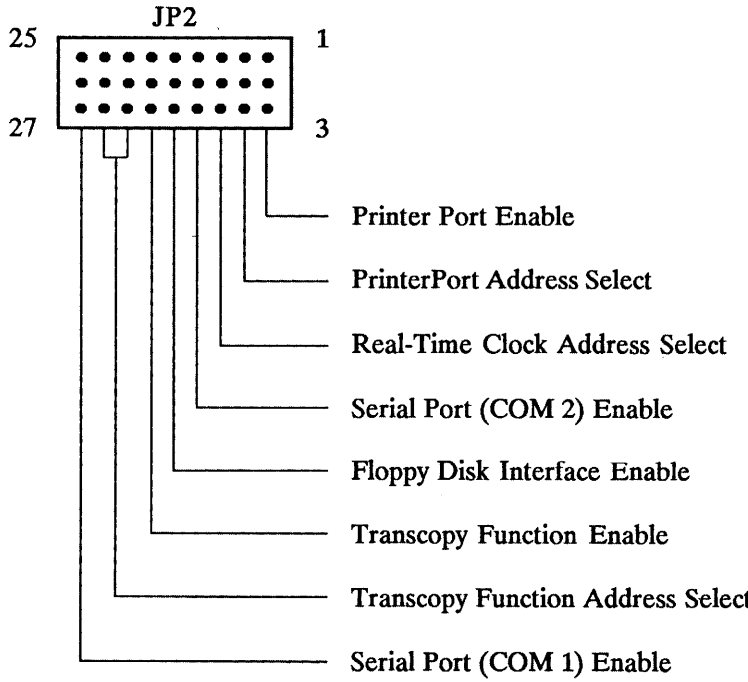
- Connectors J3 and J4, 26 ways header wafer connectors, are connectors of the two RS232C Serial Interface Ports. J3 is for the Primary Port (COM1) and J4 is for the Secondary Port (COM2). The signals on these connectors are carried to the back of the computers via the cable(s) supplied.

- Connector J5, a 34 ways header wafer connector, is for connecting to floppy disk drives.

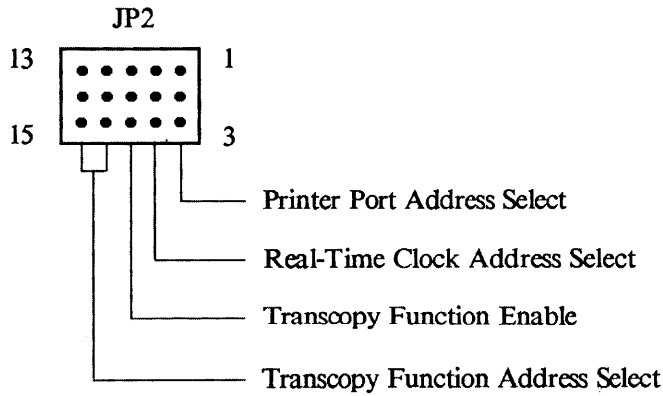
- JP1, a 4 pins jumper block, is for selecting the two different interrupt request levels for the Real-Time Clock.



JP2, a 27 pins jumper block on newer versions of the card, is a configuration Jumper Block which allows the user to select different addresses for some of the I/O functions. Moreover, some I/O functions can be disabled in case of address conflict with other devices in the system.



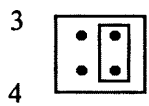
On some earlier version of the Multi-I/O Card, JP2 is a 15 pins jumper block which serves similar purpose as that on the newer version. The Floppy Disk Interface, Parallel Port, RS232C Serial Interface Ports are hardwired to be enabled.



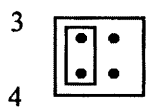
2.3 JUMPER SETTINGS

Various combinations of the jumper block and their meanings are summarized as follows. The jumpers irrelevant to the function under consideration are omitted for clarity.

Jumper Block JP1

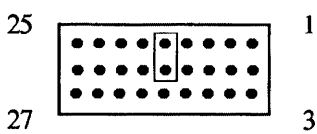


Selects Interrupt Level 2

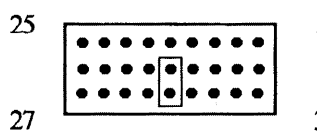


Selects Interrupt Level 5

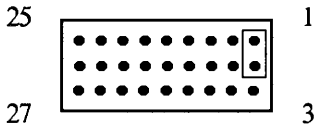
Jumper Block JP2 (on newer versions)



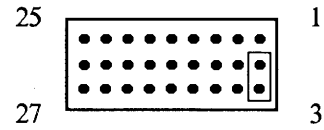
Floppy Disk
Interface Disabled



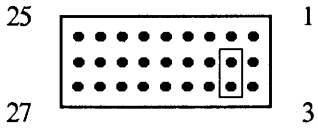
Floppy Disk
Interface Enabled



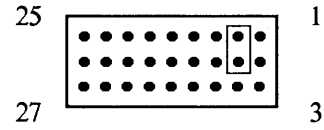
Parallel Printer
Port Disabled



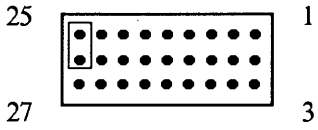
Parallel Printer
Port Enabled



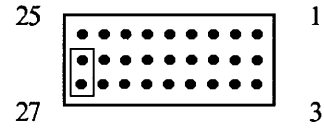
Printer Port
Address = 378-37A
(Hex)



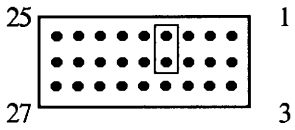
Printer Port
Address = 3BC-3BE
(Hex)



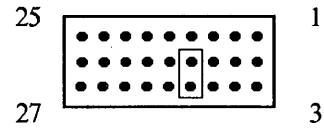
Serial Port (COM 1)
Disabled



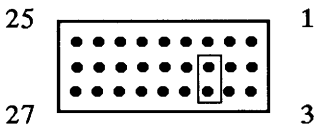
Serial Port (COM1)
Enabled



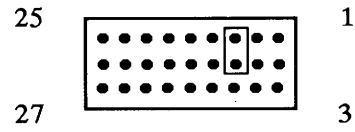
Serial Port (COM2)
Disabled



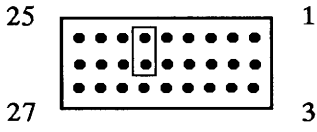
Serial Port (COM2)
Enabled



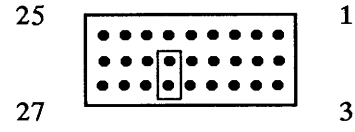
Select Real-Time Clock
Address = 340-35F (Hex)



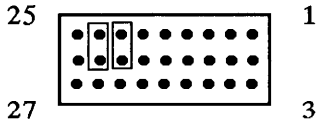
Select Real-Time Clock
Address = 2C0-2DF (Hex)



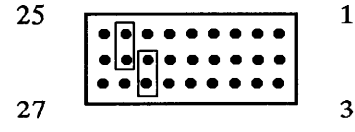
Transcopy Function
Disabled



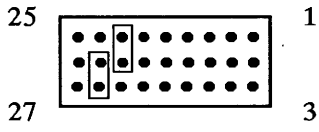
Transcopy Function
Enabled



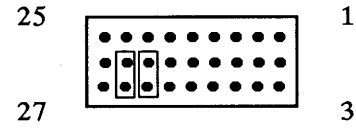
Transcopy Function
Address = 7EF (Hex)



Transcopy Function
Address = 76F (Hex)

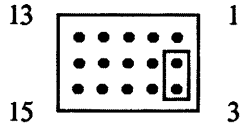


Transcopy Function
Address = 6EF (Hex)

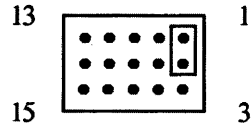


Transcopy Function
Address = 66F (Hex)

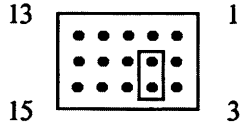
Jumper Block JP2 (on earlier version)



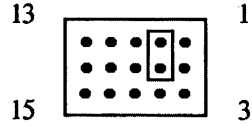
Printer Port
Address=378-37A (Hex)



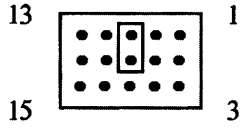
Printer Port
Address=3BC-3BE (Hex)



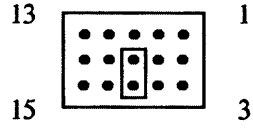
Select Real-Time Clock
Address=340-35F (Hex)



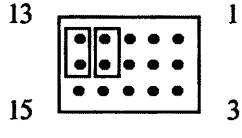
Select Real-Time Clock
Address=2C0-2DE (Hex)



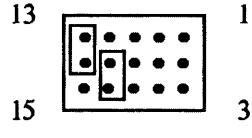
Transcopy Function
Disabled



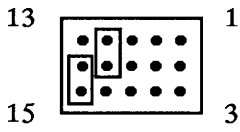
Transcopy Function
Enabled



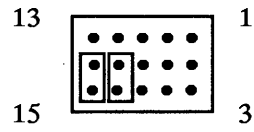
Transcopy Function
Address=7EF (Hex)



Transcopy Function
Address=76F (Hex)



Transcopy Function
Address=6EF (Hex)



Transcopy Function
Address=66F(Hex)

CHAPTER 3

HARDWARE DESCRIPTION

3. HARDWARE DESCRIPTION

This chapter describes the hardware structure of the Multi-I/O Card in terms of each function available. For a detail circuit diagram, component layout and component location list, please refer to the Appendix.

3.1 OVERALL BLOCK DIAGRAM

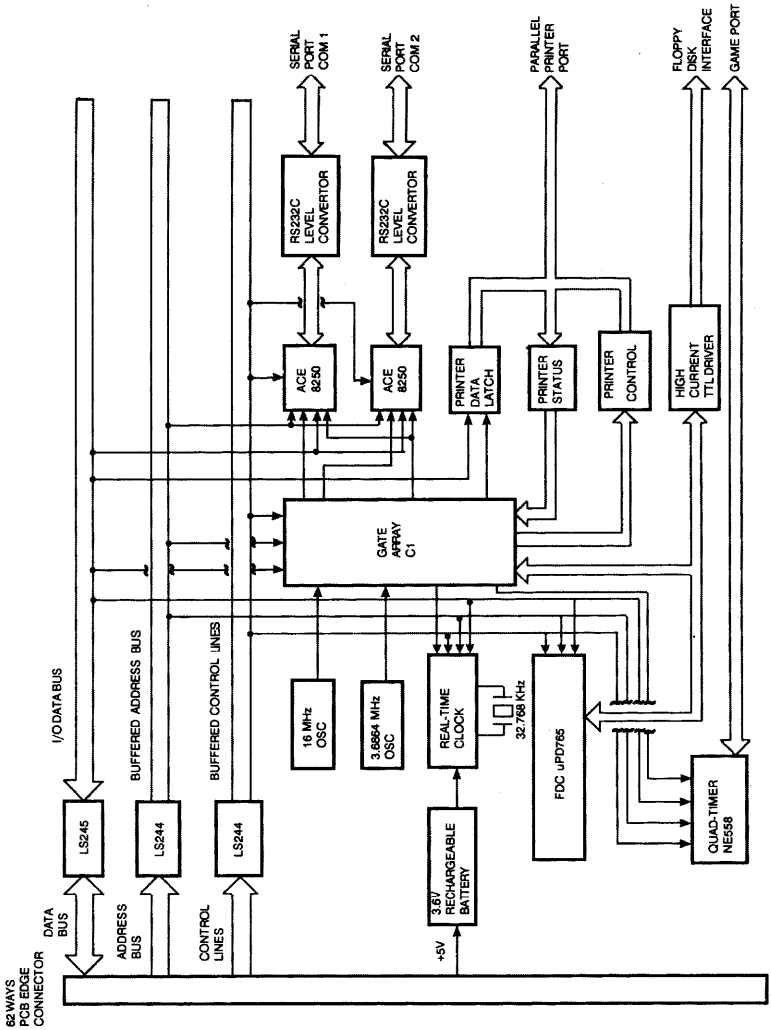


Fig . 3.1 Overall structure

The heart of the Multi-I/O Card is a 100 pins flat package Very Large Scale Integration (VLSI) Gate Array C1 (C1 is the code name used by the manufacturer for this particular chip and it will be used throughout this document).

The Gate Array C1 incorporates the hardware logic of :

- Floppy disk interface support logic for the external Floppy Disk Controller Chip uPD765 or compatibles.
- One Centronics Parallel Printer Interface.
- Address decoder and clock generator for two RS232C Serial Ports.
- Address decoder for Joystick/Game Port.
- Address decoder for Real-Time Clock chip.
- Logic for backup of protected floppy diskette (Transcopy Function).

Complete functions on the Multi-I/O Card are formed by addition of external LSI chips, buffers, latches, clock generators, battery and the required connectors.

Please refer to Chapter 4 for a complete specification of the Gate Array C1.

3.2 FLOPPY DISK INTERFACE AND TRANSCOPY FUNCTION

The floppy disk interface on the Multi-I/O Card is designed for double-sided, double-density, MFM-coded floppy disk drive. Up to two 5-1/4" double-sided, double-density floppy disk drives are supported. 3-1/2", 720K, double-sided disk drives with the same data rate and suitable device driver program will also work with the Multi-I/O Card.

3.2.1 Hardware

The floppy disk interface section includes a Floppy Disk Controller (FDC) chip uPD765, several high current TTL drivers and some logic circuitry inside the Gate Array C1. The following block diagram illustrates the structure.

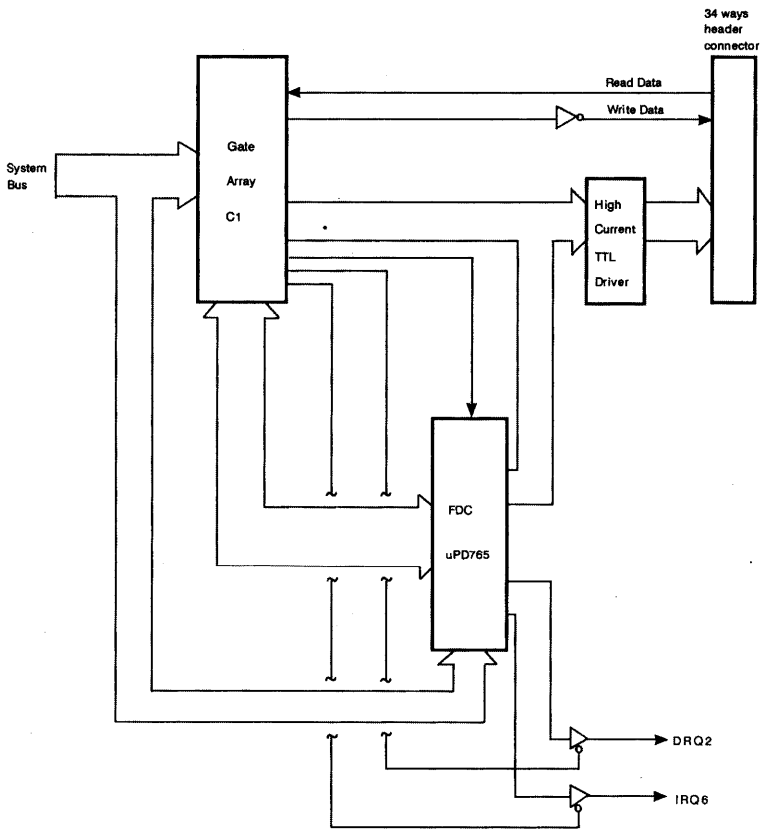


Fig. 3-2 Floppy Disk Interface

The disk drive parameters of the NEC uPD765 or compatible FDC are programmable. Transfer of data between the system memory and floppy disk controller is accomplished by Direct Memory Access (DMA) channel 2. An interrupt level 6 is also used to indicate when an operation is completed and a status condition requires processor attention.

The floppy disk interface employs write precompensation for its record data to improve reliability. Write pre-compensation is controlled by the FDC (uPD765) and performed inside the Gate Array C1. Write pre-compensation constant of 250ns using a 4MHz clock is implemented.

Data recovery of the MFM raw read data from floppy disk drive is done by a digital data separator built inside the Gate Array C1. The digital data separator is a synchronous counter type employing a 16MHz reference clock for higher reliability margin in the separated data.

The hardware logic of Transcopy is built entirely inside the Gate Array C1. This part includes a control port, serial to parallel convertor, parallel to serial convertor, status port, data / clock pulse generator and their associated address decoder. When the Transcopy function is activated via proper software, the reading / writing of floppy disk data will go directly through the Transcopy logic and the FDC uPD765 is bypassed. This enables the Transcopy function to resolve the copy-protection schemes used by most software packages. The Transcopy logic uses DMA channel 2 for its operation.

3.2.2 Programming Considerations

The floppy disk interface presents a high level command interface to software I/O drivers. From a programming point of view, the interface consist of an 8-bit digital-output register plus a uPD765 or compatible floppy disk controller. The following table shows the I/O Address used.

Register	I/O Address Used (Hex)
FDC Data Register	3F5
FDC Main Status Register	3F4
Digital Output Register	3F2

The floppy disk controller (FDC) contains two registers that may be accessed by the system processor: a status register and a data register. The 8-bit main status register contains the status information of the FDC and may be accessed at any time. The 8-bit data register stores data, commands, parameters, and provides floppy drive status information.

The FDC is capable of executing 15 different commands, each initiated by a multi-byte transfer from the processor. The results of command execution is also a multi-byte transfer back to the processor. Each command can be broadly divided into three phases:

- Command Phase
- Execution Phase
- Result Phase

Please refer to the data sheet of FDC uPD765 in the Appendix for details of these command descriptions.

The digital output register (3F2) is an output-only register used to control drive motors, drive selection and feature enable. All bits are cleared by the I/O interface reset line. The hardware logic for this register, together with other address decoding and DMA support logic, are all built inside the Gate Array C1.

The bits in the digital output register have the following functions:

Bits 0,1 Decoded by hardware to select one drive.

Bit 1	Bit 0	Drive Selected
0	0	0 (A)
0	1	1 (B)
1	0	Not applicable
1	1	Not applicable

Bit 2 The FDC (uPD765) is reset when this bit is clear. It must be set by program to enable the FDC.

Bit 3 This bit, when set, allows the FDC interrupt and DMA request to be gated onto the System Bus. When cleared, interrupt and DMA cannot be generated.

Bit 4,5 These bits controls, respectively, the spindle motors of drive 0 (A) and 1 (B). If they are set while the associated drive is selected, that motor will be turned on. Otherwise, it is off.

Bit 6, 7 Not used.

The Transcopy hardware appears to the programmer as a single Read/Write I/O port. The address of this I/O port is 7EF/76F/6EF/66F depending on the current jumper block settings.

Bit definitions are as follows:

When CPU write:

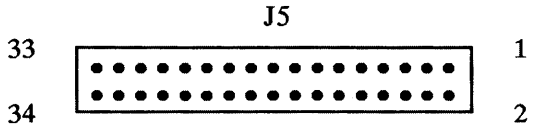
Bit 0	Transcopy DMA (channel 2) enable.
Bit 1	Transcopy Read control.
Bit 2	Transcopy Write control.
Bits 3,4,5	Internal Counter control.
Bits 6,7	Transcopy Data Rate control.

When CPU read:

Bits 0-5	Not used (garbage).
Bit 6	Value of Bit 7 on a previous CPU write operation to this I/O port.
Bit 7	Index signal from floppy disk drive.

All bits are cleared by system reset.

3.2.3 Connector Pin Assignment



Pin No.	Function
1-33 (odd no.)	Ground
2,4,6,34	Unused
8	Index
10	Motor Enable A
12	Drive Select B
14	Drive Select A
16	Motor Enable B
18	Direction (Stepper Motor)
20	Step Pulse
22	Write Data
24	Write Enable
26	Track 0
28	Write Protect
30	Read Data
32	Select Head 1

3.3 PARALLEL PRINTER PORT

The parallel printer port on the Multi-I/O card is a Centronics type parallel port. This type of parallel port can be used as a general input / output port for any device or application that matches its signal input / output specification.

3.3.1 Hardware

Functional block diagram of the parallel printer port is as follows:

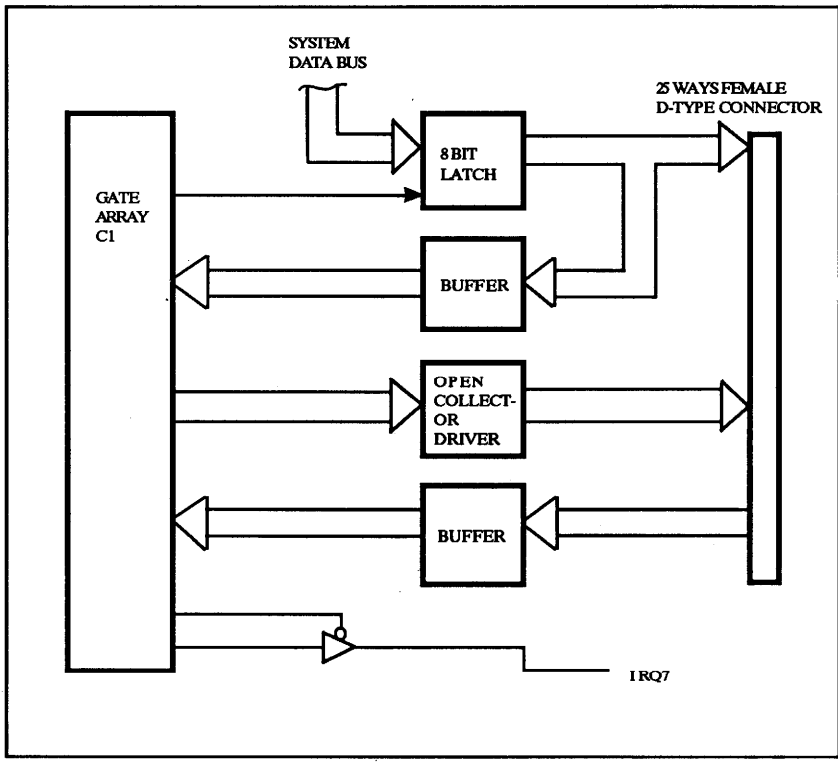


Fig. 3.3 Parallel Printer Port

8 bit data are output to the parallel device by writing to an 8-bit register, while status signals can be read through a status register. An input line (ACK) can be used to create an interrupt to the processor when it is properly enabled.

Most of the necessary hardware logic and decoding are built inside the Gate Array C1. Externally, an 8-bit data latch, which also serves as signal driver, plus some open collector drivers and buffer, are needed.

3.3.2 Programming Considerations

The parallel printer port uses I/O Address 378-37A (Hex) or 3BC-3BE (Hex), depending on the current jumper block setting. The hardware appears as registers / latches accessible by the system processor.

I/O Address (Hex)	Function
378/3BC	Printer Data Port
379/3BD	Printer Status Port
37A/3BE	Printer Control Port

Parallel Data Port 378 / 3BC:

This is an 8-bit read/write parallel data port for the parallel external device. The signal is held stable by latches and can be read back any time via the same I/O Address.

Printer Status Port 379 / 3BD:

This is a read only status port which can be accessed by the CPU to check for status of the external parallel device.

Bit Number	Status
0	Not used
1	Not used
2	Not used
3	Not used
4	SLCT
5	PE
6	ACK
7	BUSY

Printer Control Port 37A / 3BE:

The Printer control port, when written to, presents the following latched control signals to the external parallel device:

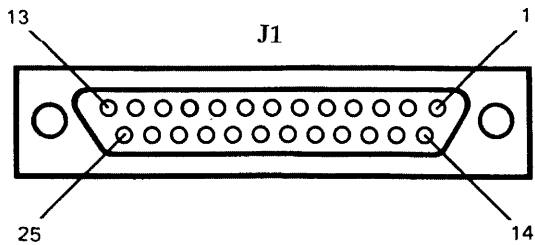
Bit Number	Control Signal
0	$\overline{\text{STROBE}}$
1	$\overline{\text{AUTO FD}}$
2	$\overline{\text{INIT}}$
3	$\overline{\text{SLCTIN}}$
4	IRQ7 Enable
5	Not used
6	Not used
7	Not used

The status of the control signals output being latched by a previous write command to I/O port 37A/3BE, can be read from the same address.

Bit Number	Status of Control Signal
0	$\overline{\text{STROBE}}$
1	$\overline{\text{AUTOFD}}$
2	$\overline{\text{INIT}}$
3	$\overline{\text{SLCTIN}}$
4	Not used
5	Not used
6	Not used
7	Not used

System interrupt level 7 can be enabled by setting bit 4 in the Printer Control Port (37A / 3BE) and activating the $\overline{\text{ACK}}$ input line.

3.3.3 Connector Pin Assignment

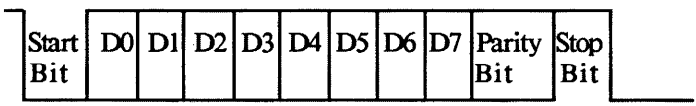


Pin No	Function
1	$\overline{\text{STROBE}}$
2	Parallel Data D0
3	Parallel Data D1
4	Parallel Data D2
5	Parallel Data D3
6	Parallel Data D4
7	Parallel Data D5
8	Parallel Data D6
9	Parallel Data D7
10	$\overline{\text{ACK}}$
11	BUSY
12	PE
13	$\overline{\text{SLCT}}$
14	$\overline{\text{AUTO FD}}$
15	$\overline{\text{ERROR}}$
16	$\overline{\text{INIT}}$
17	$\overline{\text{SLCTIN}}$
18-25	GROUND

3.4 RS232C SERIAL INTERFACE PORTS

The Multi-I/O card supports up to two RS232C Serial Interface Ports. They are designated as COM1 and COM2 in accordance with their I/O Address 3F8-3FF (Hex) and 2F8-2FF (Hex) respectively. These serial ports provide interface for serial devices including modem, serial printer and terminal.

The serial communication ports are fully programmable and supports asynchronous communications only. They add and remove start bits, stop bits and parity bits. A programmable baud rate generator allows operation from 50 baud to 9600 baud. Five, six, seven or eight bit characters with 1, 1-1/2 or 2 stop bits are supported.



Each serial port has it assigned level of system interrupt. A fully prioritized interrupt system within each serial port controls transmit, receive, error, line status and data set interrupts. Diagnostic capabilities provide loopback functions of transmit / receive and input / output signals.

3.4.1 Hardware Description

Following is a block diagram of hardware for one serial port (COM1).

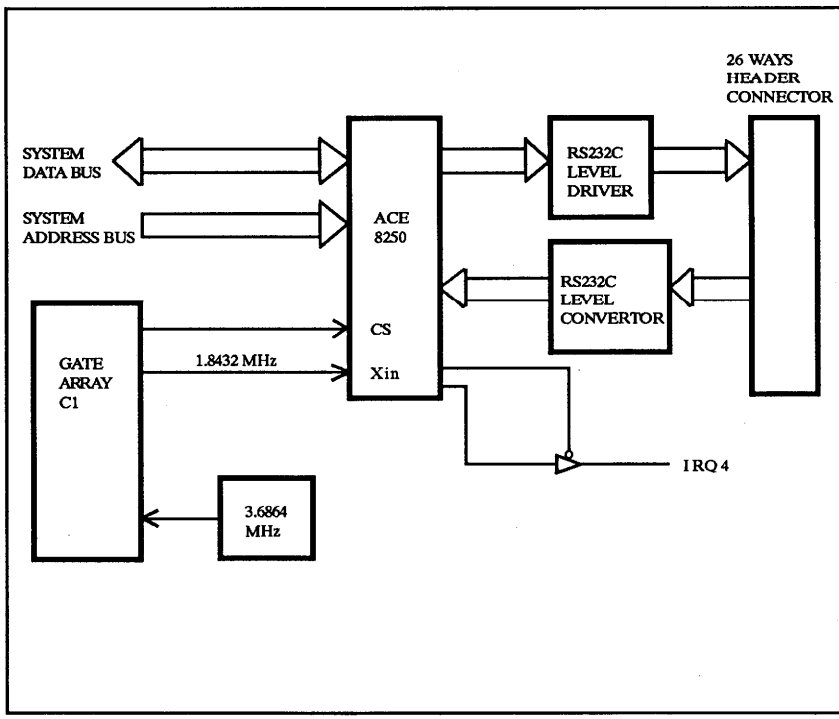


Fig. 3.4 RS232C Serial Interface Port

The heart of the Serial Communication Port is the INS8250 Asynchronous Communication Element (ACE), or its functional equivalent . Address decoding and clock generation is done in Gate Array C1. A 3.6864MHz signal input to Gate Array C1 is divided by two and fed to the INS8250 ACE chip as a 1.8432 MHz master clock. Baud rates of 50 to 9600 are generated from this 1.8432 MHz signal.

The serial data output, together with modem control output from the ACE, are changed from TTL voltage into RS232C voltage levels via signal drivers 1488 or equivalent. Conversely, RS232C voltage levels are converted back to TTL levels by signal converters 1489 or equivalent and fed to the ACE inputs.

3.4.2 Programming Considerations

Apart from the general function listed above, the ACE also features:

- Full double buffering eliminates extra hardware / software for precise synchronization.
- Modem control functions of Clear to Send (CTS), Request to Send (RTS), Data Set Ready (DSR), Data Terminal Ready (DTR), Ring Indicator (RI), and Carrier Detect.
- False - start bit detection.
- Line - break generation and detection.

The INS8250 ACE is fully programmable for each function and any communication protocol must be loaded before the serial port is operational. This is done by selecting the proper I/O Address for each Serial Port. The following tables summarizes the I/O Address assigned to the internal registers of INS8250 ACE in the Multi-I/O card. The divisor latch access bit DLAB (bit7) of the line control register is used to select certain register.

I/O Decode (in Hex)		Register Selected	DLAB State
COM1	COM2		
3F8	2F8	TX Buffer	DLAB=0(Write)
3F8	2F8	RX Buffer	DLAB=0(Read)
3F8	2F8	Divisor Latch LSB	DLAB=1
3F9	2F9	Divisor Latch MSB	DLAB=1
3F9	2F9	Interrupt Enable Register	
3FA	2FA	Interrupt Identification Registers	
3FB	2FB	Line Control Register	
3FC	2FC	Modem Control Register	
3FD	2FD	Line Status Register	
3FE	2FE	Modem Status Register	

I/O Decodes

Hex Address 3F8 to 3FF and 2F8 to 2FF											
A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	DLAB	Register
1	1/0	1	1	1	1	1	X	X	X		
							0	0	0	0	Receive Buffer (read) Transmit Holding Reg (write)
							0	0	1	0	Interrupt Enable
							0	1	0	X	Interrupt Identification
							0	1	1	X	Line Control
							1	0	0	X	Modem Control
							1	0	1	X	Line Status
							1	1	0	X	Modem Status
							1	1	1	X	None
							0	0	0	1	Divisor Latch (LSB)
							0	0	1	1	Divisor Latch (MSB)

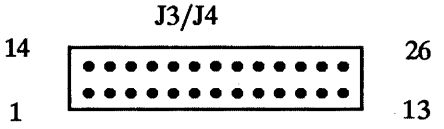
Address Bits

Note: Bit 8 will be logical 1 for the port designated as COM1 or a logical 0 for the port designated as COM2.

A2, A1 and A0 bits are used to select the different register of the communications chip.

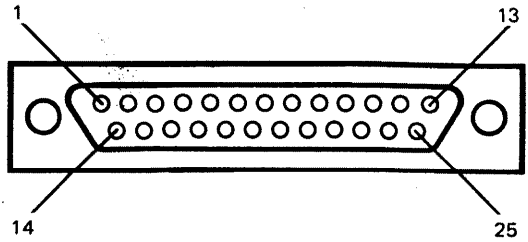
Please refer to the data sheet of ACE INS8250 in the Appendix for details of these internal registers.

3.4.3 Connector Pin Assignment



Pin No.	Function
1	Ground
2	TX
3	RX
4	RTS
5	CTS
6	DSR
7	Ground
8	RLSD
9-19	Not used
20	DTR
21	Not used
22	RI
23-26	Not used

DB25 male connector on bracket



Pin No.	Function
1	Ground
2	TX
3	RX
4	RTS
5	CTS
6	DSR
7	Ground
8	RLSD
9-19	Not used
20	DTR
21	Not used
22	RI
23-25	Not used

3.5 GAME PORT

The Game Port on the Multi-I/O Card allows up to four game paddles or two joysticks to be attached. In addition, inputs for four switch buttons are provided. Paddle and joystick positions are determined by the variable resistance values sensed by the Joystick/ Game Port. The real-time resistive values are converted into a relative paddle or joystick position via appropriate software.

3.5.1 Hardware

The following is the block diagram of the joystick / game port.

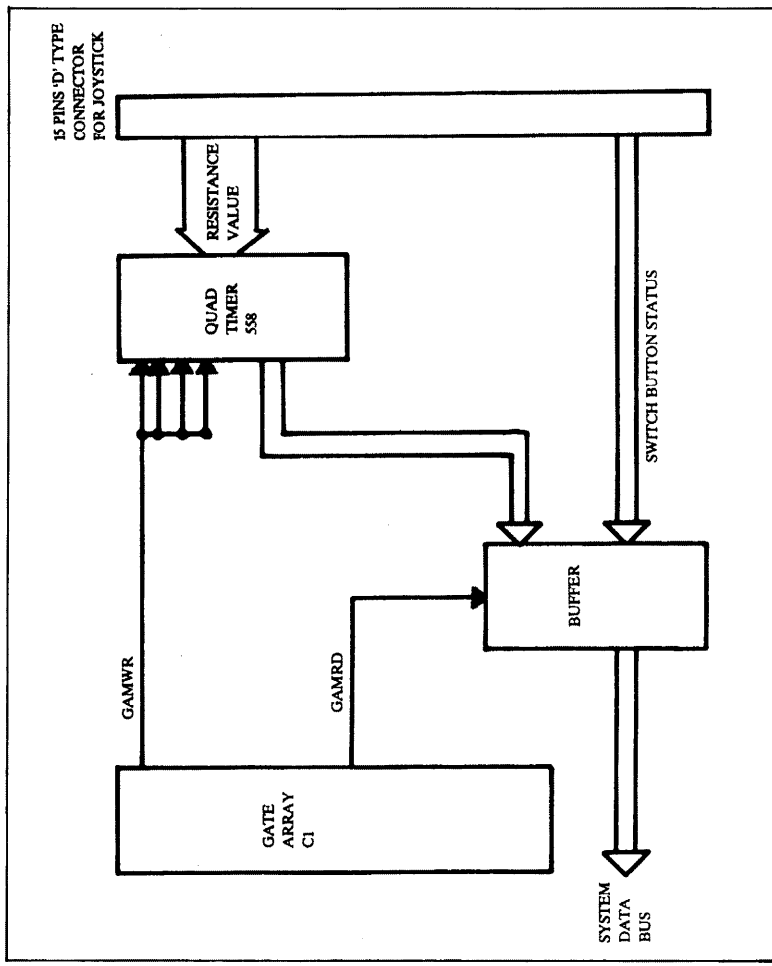


Fig. 3.5 Joystick/Game Port

The chip for conversion of resistance value into digital state is the Quad-Timer NE558 or equivalent. Address decoding for the Joystick / Game Port is provided by the Gate Array C1. I/O Address

for triggering of four monostable timers as well as reading of position / button status byte is 201 Hex. The position/button status are gated via data buffer with its enable line decoded from Gate Array C1.

3.5.2 Programming Considerations

The Joystick / Game Port appears to the programmer as one Read/ Write Port with I/O Address 201 Hex.

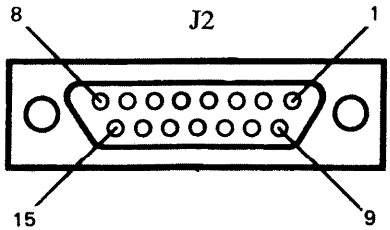
When an I/O write command is issued to port address 201 Hex, irrespective of the data written, all four monostable outputs go high and will remain high for varying periods of time depending on the position each variable resistor of the joystick is set. The variable resistance on the joystick should have a range from 0 to 100K-ohms.

These four monostable timer outputs are read by an I/O read command from port address 201 Hex and are reflected on data bits 0 through 3.

Bit 4 through 7 of the I/O port reflects the real-time status of the switch buttons. These buttons default to an open state and are read as "1". When a button is pressed, it is read as "0:". Programmers should note that these buttons are not debounced by hardware.

Bit Number	Function
0	Position 0
1	Position 1
2	Position 2
3	Position 3
4	Switch Button 0
5	Switch Button 1
6	Switch Button 2
7	Switch Button 3

3.5.3 Connector Pin Assignment



Pin No.	Function
1	+5V DC
2	Button 0
3	Position 0
4	Ground
5	Ground
6	Position 1
7	Button 1
8	+5V DC
9	+5V DC
10	Button 2
11	Position 2
12	Ground
13	Position 3
14	Button 3
15	+5V DC

3.6 REAL-TIME CLOCK

The Multi-I/O Card is equipped with a Real-Time Clock and re-chargeable battery backup. This function maintains the time and calendar, and, with suitable software, allows automatic setting up of time and date each time the computer is turned on.

3.6.1 HARDWARE

Following is a block diagram of the Real-Time Clock.

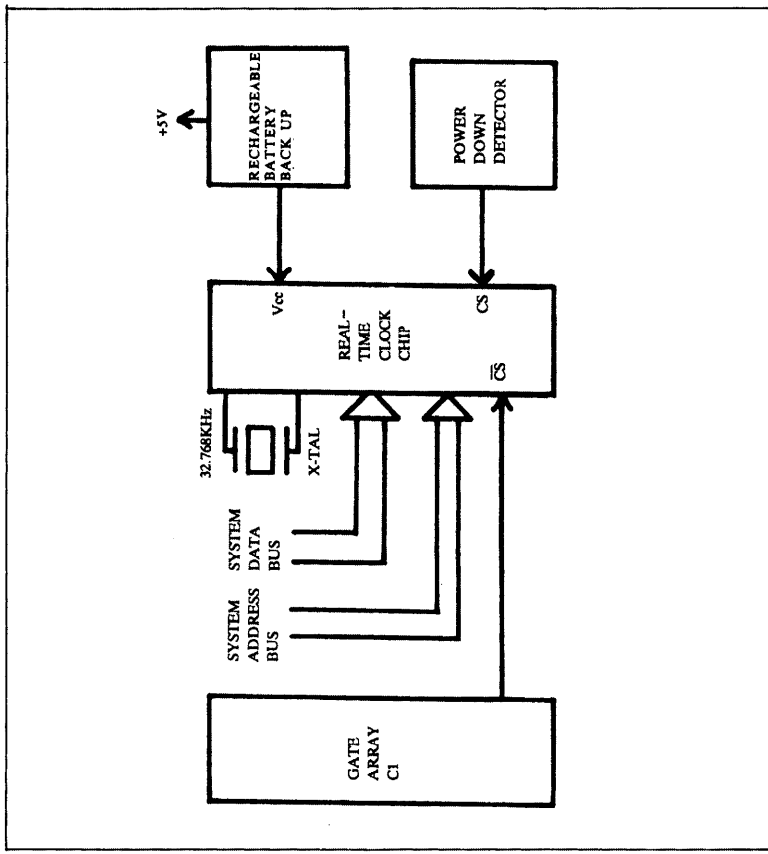


Fig. 3.6 Real-Time Clock

The heart of the Real-Time Clock is the real-time clock chip. The Multi-I/O Card has made provision to work with two different real-time clock chips, namely, the OKI MSM 6242 or the RICOH RP5C15. These chips are on different locations of the PCB.

The real-time clock chip runs with a clock of 32.768 KHz for its internal counting operation.

This chip normally draws power from the computer's +5V supply when the computer is turned ON. The backup battery is recharged from the +5V supply. When the power is OFF, the backup battery replaces the normal +5V to keep the chip running.

A power down detection circuitry is added to pull the CS line of the real-time clock chip to logic low as soon as the computer's +5V supply is dropping. This prevents transient garbage to be written to the chip during power down.

Address decoding for the real-time clock chip is done in Gate Array C1. The I/O Address range used is 340-35F (Hex) or 2C0 - 2DF (Hex), depending on the current jumper block setting.

3.6.2 Programming Considerations

The Real-Time Clock function appears to the programmer as a number of CPU addressable registers. These registers serve functions including second, minute, hour, day, month, year and days of the week.

The real-time clock chip incorporates 16 such registers, while the Gate Array C1 decodes 32 different addresses. The upper 16 addresses map to the lower 16 addresses.

The Real-Time Clock utility programs SETCLOCK,GETCLOCK supplied with the card automatically handle the different chips used and different addresses selected.

Refer to the Appendix for detail meaning of the real-time clock chip registers.

CHAPTER 4

GATE ARRAY C1

CHAPTER 4
GATE ARRAY C1

The Gate Array C1 is a 100 pins flat package VLSI Gate Array designed to implement a number of I/O functions for the IBM®PC, PC/XT and compatibles.

It consists of the logic circuitry for the following popular I/O features:

- Floppy disk interface support logic for the Floppy Disk Controller Chip uPD765.
- One Centronics Parallel Printer Interface.
- Address decoders for two RS232C Serial ports.
- Address decoder of a Joystick/Game Port
- Address decoder for a Real-Time Clock Chip.
- Logic circuitry for backup of copy-protected diskette (Transcopy Function).

4.1 FUNCTIONAL BLOCK DIAGRAM

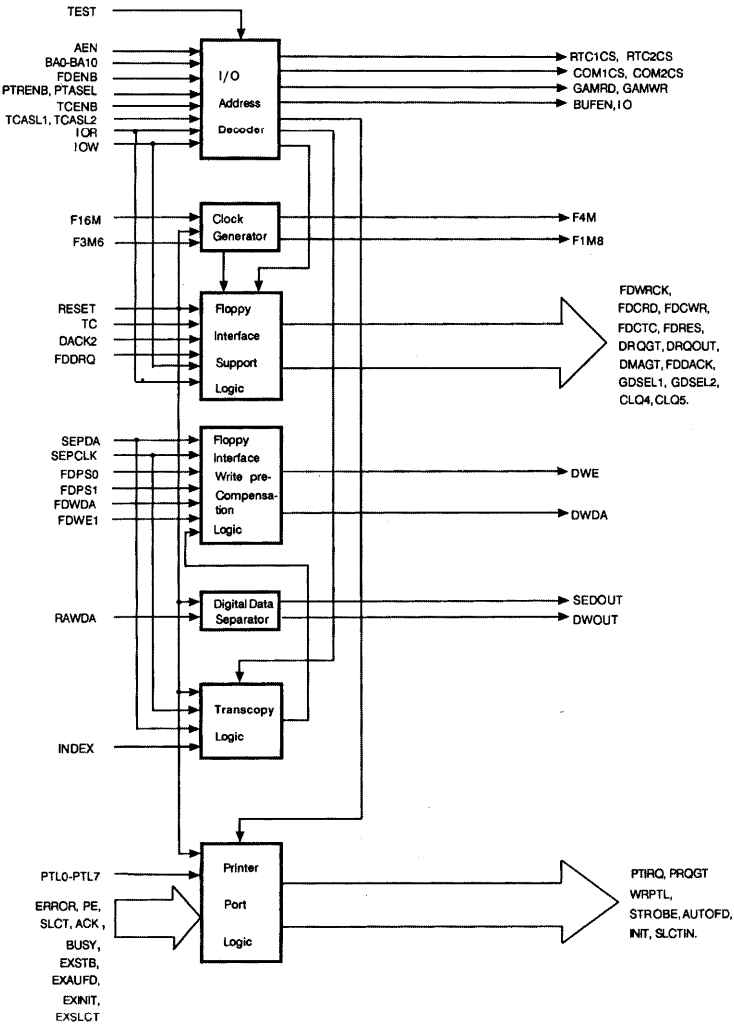


Fig 4.1 Gate Array C1 Function Diagram

4.2 PIN ASSIGNMENT AND SIGNAL DESCRIPTION

Abbreviation on pin type:

I	Input
O	Output
I/O	Bi-directional

Pin No.	Pin type	Name	Description
1	I	PTRENB	Printer Port enable line. Active high input. 1=printer port enabled 0=printer port disabled
2	I	PTASEL	Printer Port I/O address select. 1=378-37A (Hex) 0=3BC-3BF (Hex)
3	O	RTC1CS	Real-Time Clock 1 address decoder. Active low output. Address range=340-35F (Hex)
4	/	N.C.	No connection.
5	O	RTC2CS	Real-Time Clock 2 address decoder. Active low output. Address range=2C0-2DF (Hex)
6	O	COM1CS	RS232C Serial Port 1 address decoder. Active low output. Address range=3F8-3FF (Hex)
7	O	COM2CS	RS232C Serial Port 2 address decoder. Active low output. Address range=2F8-2FF (Hex)

8	I	FDENB	Floppy Disk Interface enable. Active low input. 0=Floppy Interface enabled 1=Floppy Interface disabled
9	I	TCENB	Transcopy Function enable. Active high input. 1=Transcopy Function enabled 0=Transcopy Function disabled
10	I	TCASL1	Transcopy Function address select 1.
11	I	TCASL2	Transcopy Function address select 2. Different combinations of TCASL1, TCASL2 results in one of four possible addresses for Transcopy Function:

TCASL2	TCASL1	I/O Address
0	0	7EF
0	1	76F
1	0	6EF
1	1	66F

12	I	F3M6	Input signal from an external 3.6864MHz oscillator. The signal is divided by 2 in Gate Array C1 to generate a 1.8432MHz output signal for the serial communication chips.
13	I	F16M	Input signal from an external 16MHz oscillator. All necessary timing signal for the Floppy Disk Interface are derived from this 16MHz signal.

14	O	GDSEL2	Partially decoded Drive B select signal for the Floppy Disk Interface. Active high output. This signal should be NAND with CLQ5 to produce the valid Drive B select signal.
15	/	GND	0 V
16	O	GDSEL1	Partially decoded Drive A select signal for the Floppy Disk Interface. Active high output. This signal should be NAND with CLQ4 to produce the valid Drive A select signal.
17	O	CLQ4	Motor enable signal for floppy disk drive A. Active high output.
18	O	CLQ5	Motor enable signal for floppy disk drive B. Active high output.
19	O	DWE	Floppy drive write enable signal. Active high output.
20	O	DWDA	Floppy drive write data signal. Active high output.
21	O	IO	This signal is a logical AND of the IOR, IOW. Active low output, indicating I/O Read, I/O Write is in progress.
22	O	F1M8	This signal is a 1.8432MHz square wave output signal derived from the 3.6864MHz input signal.

23	O	F4M	This is a 4MHz square wave output derived from the 16MHz input signal. This signal is used as the clock input of an external FDC uPD765, or as the reference clock in an external data separator WD9216.
24	O	FDCWR	Decoded output signal to the Write input of an external FDC uPD765. Active low output. This line is activated when the CPU writes to the FDC or DMA write to the FDC is in progress.
25	O	FDCRD	Decoded output signal to the Read input of an external FDC uPD765. Active low output. This line is activated when the CPU reads from the FDC or DMA read from the FDC is in progress.
26	O	FDCTC	Terminal count output to an external FDC uPD765. Active high output. This line is activated at the end of each DMA transfer for Floppy Disk Interface.
27	/	N.C.	No connection.
28	O	FDWRCK	Write clock output to an external FDC uPD765. 500 KHz positive going pulse signal.
29	O	FDRES	Reset output to an external FDC uPD765. Active high output. This line is activate when a "0" is written to the Digital Output Register (Hex 03F2) of the Floppy Disk Interface inside the Gate Array.

30	O	DRQGT	Control output for Floppy Disk Interface DMA Request. Active low output. This line is used for enabling an external tri-state buffer (LS125) which has output driving the system DMA Request channel 2.
31	O	DRQOUT	Floppy Disk Interface DMA Request. Normally tri-state with active high output. This line is connected to a tri-state buffer (LS125) which drives the system DMA Request channel 2.
32	O	DMAGT	Control output for Floppy Disk Interface Interrupt Request. Active low output. This line is used for enabling an external tri-state buffer (LS125) which has input from the uPD765 Interrupt line, and drive the system IRQ level 6.
33	I	FDPS0	Floppy Disk Interface Write Precomp 0.
34	I	FDPS1	Floppy Disk Interface Write Precomp 1. FDPS0,FDPS1 are input signals from an external FDC uPD765. These two signals controls the amount of write pre- compensation to be effected on the write data to floppy disk drive. Maximum write pre-compensation is +/-250nS.
35	I	TC	System Terminal Count. Active high input.
36	O	SEDOUT	Separated Data out. Active low output from an internal digital data separator inside the Gate Array. The active duration of the pulse output is 62.5nS.

37	O	DWOUT	Data Window out. This is a 250KHz rectangular wave output from the internal digital data separator inside the Gate Array. The phase (edges) of this signal will shift back and forth according to the raw read data from the floppy disk drive.
38	I	SEPDA	Separated Data input. This is the separated read data for use by Floppy Disk Interface and the Transcopy Function. If the internal digital data separator is used, this pin should be connected to the SEDOUT (pin 36) of the Gate Array. If an external data separator is adopted, this pin should be connected to the separated data output from the external data separator.
39	I	SEPCLK	Separated Clock input. This is the separated clock, or the data window used by the Floppy Disk Interface and the Transcopy Function. If the internal digital data separator is used, this pin should be connected to the DWOUT (pin 37) of the same Gate Array. If an external data separator is adopted, this pin should be connected to the separated clock, or data window output from the external data separator.
40	I	FDWE1	Floppy disk drive write enable. Active high input from an external FDC uPD765.
41	/	VCC	+5V DC supply voltage.
42	I	FDWDA	Floppy disk write data. Active high input from an external FDC uPD765. This write data is not yet write pre-compensated.

43	O	FDDACK	Floppy Disk Interface DMA Acknowledge. Active high output signal to an external FDC uPD765.
44	I	FDDRQ	Floppy Disk Interface DMA Request. Active high input signal from an external FDC uPD765.
45	I	RAWDA	Raw read data from floppy disk drive. Active low input which is used by the internal digital data separator.
46	O	PTIRQ	Printer Port interrupt request. Tri-state normally, high when active. This pin should connect to a tri-state buffer (LS125) which drives the system Interrupt level 7.
47	O	PRQGT	Printer Port interrupt request control. Active low output. This pin should be used for controlling a tri-state buffer (LS125) which drives the system Interrupt level 7.
48	I	ERROR	Printer status signal - ERROR.
49	I	INDEX	Floppy disk drive Index signal. Active low input. This signal is used by the Transcopy logic inside the Gate Array.
50	I/O	BD0	Data line D0
51	I/O	BD1	Data line D1
52	I/O	BD2	Data line D2
53	I/O	BD3	Data line D3

54	I/O	BD4	Data line D4
55	I/O	BD5	Data line D5
56	I/O	BD6	Data line D6
57	I/O	BD7	Data line D7
58	I	AEN	System Address Enable. Active low input. All CPU Read/Write takes place when AEN is active.
59	I	IOR	System I/O Read. Active low input.
60	I	IOW	System I/O Write. Active low input.
61	I	DACK2	System DMA channel 2 Acknowledge. Active low input.
62	I	RESET	System Reset. Active high input.
63	I	BA0	Address line A0
64	I	TEST	Test input for factory diagnostic purpose. Must be grounded (tie to 0 V) for normal operation.
65	/	GND	0 V
66	I	BA1	Address line A1
67	I	BA2	Address line A2
68	I	BA3	Address line A3
69	I	BA4	Address line A4
70	I	BA5	Address line A5
71	I	BA6	Address line A6

72	I	BA7	Address line A7
73	I	BA8	Address line A8
74	I	BA9	Address line A9
75	I	BA10	Address line A10
76	O	STROBE	Printer control output - STROBE
77	O	AUTOFD	Printer control output - AUTOFD
78	O	INIT	Printer control output - INIT
79	O	SLCT IN	Printer control output - SLCT IN
80	O	WRPTL	Printer Port parallel data latch signal. Active low output. Decoded address = 378/3BC (Hex)
81	I	PTL0	Printer Port parallel data 0 input
82	I	PTL1	Printer Port parallel data 1 input
83	I	PTL2	Printer Port parallel data 2 input
84	I	PTL3	Printer Port parallel data 3 input
85	I	PTL4	Printer Port parallel data 4 input
86	I	PTL5	Printer Port parallel data 5 input
87	I	PTL6	Printer Port parallel data 6 input
88	I	PTL7	Printer Port parallel data 7 input
89	O	BUFEN	Enable signal for an external data buffer (LS245) connected between the data lines of the Gate Array and the system data bus.
90	I	EXSTB	Printer status signal - STROBE
91	/	VCC	+5V DC supply voltage.
92	I	EXAUFD	Printer status signal - AUTOFD
93	I	EXINIT	Printer status signal - INIT

94	I	EXSLCT	Printer status signal - SLCT IN
95	I	SLCT	Printer status signal - SLCT
96	I	PE	Printer status signal - PE
97	I	ACK	Printer status signal - ACK
98	I	BUSY	Printer status signal - BUSY
99	O	GAMRD	Game Port Read signal. Active low output. I/O address decoded = 201 (Hex)
100	O	GAMWR	Game Port Timer Trigger. Active low output. I/O address decoded = 201 (Hex)

4.3 ELECTRICAL SPECIFICATIONS

4.3.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	Vcc	-0.3~+6.7	V
Terminal voltage	Vt	-0.3~Vcc+0.3	V
Output Current			
- per one output	Io	-8~+8	mA
- total	Iot	-40~+40	mA
Operating Temperature	Topr	-20~+75	C
Storage Temperature			
- with Bias	Tbias	-20~+85	C
- without Bias	Tstg	-55~+125	C

4.3.2 Electrical Characteristics

Vcc = 5V +/- 5%, Ta = -20°to 75°C

Parameter	Symbol	min	max	unit
Input Voltage	VIH	2.2	Vcc+0.3	V
	VIL	-0.3	0.8	V
Output Voltage	VOH	3.5		V
	(IOH = -2mA)			
	VOL		0.5	V
	(IOL = 5mA)			
Input Leakage Current	ILI		1	uA
Output Leakage Current	ILO		1	uA

4.4 MECHANICAL INFORMATION

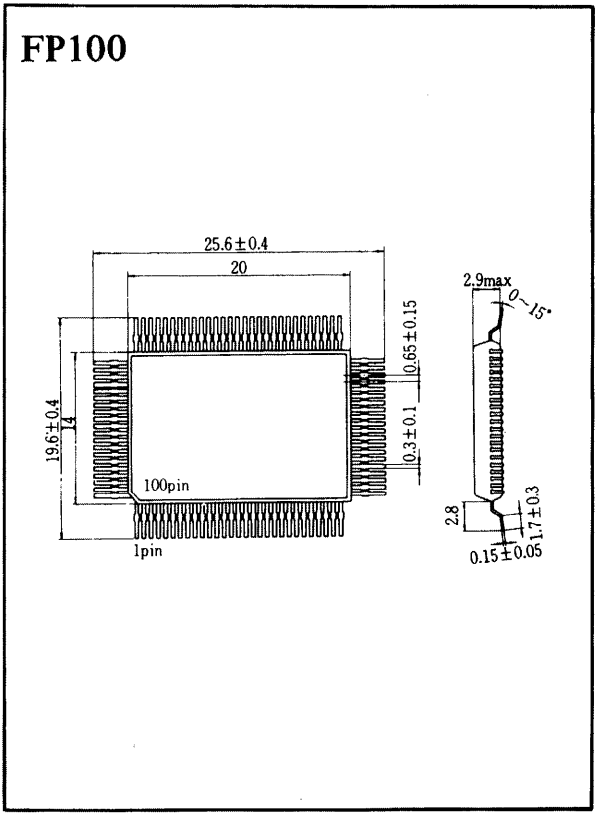


Fig 4.2 Gate Array C1

CHAPTER 5

TROUBLE - SHOOTING GUIDE

CHAPTER 5
TROUBLE-SHOOTING GUIDE

This chapter describes the general guidelines for trouble-shooting of the Multi-I/O Card.

For more detail information on logic states please refer to the Gate Array C1 Specification in Chapter 4, data sheets of various components and the circuit schematic diagrams in the Appendix.

Technical reference manual of the host main unit will also be of help.

Refer to your DOS (Disk Operating System) User's Manual for errors associated with disk I/O.

The description contained in this chapter assumes that the problem comes from, or most likely from, the Multi-I/O Card. This can easily be verified by removing the card from the system, exchange for another I/O Card, or move the suspected Multi-I/O Card to another system and observe the result. Remember to turn power OFF before removing any card.

5.1 GENERAL FAILURE

Symptom

Computer system no response after power up. Power indicator on main unit does not light up.

Possible causes	Solution
. +5V failure/ short circuited on Multi-I/O Card.	. Check for +5V DC short-circuiting on Multi-I/O Card
	. Check for short-circuited decoupling capacitor.
	. Check for short-circuited I.C. chips.
	. Check if the card is inserted properly in the main unit slot.

Symptom

Main unit power indicator lights up. Computer no video, or no other response, including the power up 'beep' sound.

Possible causes	Solution
. System address bus, data bus, or control lines contamination due to Multi-I/O Card failure.	. Check data buffer and address buffer I.C. U1,U6,U12 on Multi-I/O Card.
. Multi-I/O Card not inserted properly.	. Check if the card is inserted properly in the slot.

5.2 FLOPPY DISK INTERFACE/TRANSCOPY FAILURE

Symptom

Floppy drive not booting.

Possible causes	Solution
. Floppy drive function disabled (on newer versions of this card).	. Change jumper block setting to enable this function.
. I/O Address conflict with another floppy drive adapter on the main unit.	. Change jumper block setting to disable this function, while use the built-in adapter on the main unit.
. Data bus contamination on all I/O functions.	. Check I/O data bus buffer U1. . Check all other LSI, I.C. connected to the I/O data bus. . Check Gate Array C1 (U20).
. Floppy drive interface logic failure.	. Check FDC chip uPD765 (U27), U21,U25,U26, U30,U28,U29,U14,U30, R19,R20,R21,R22,Xtal 2.
. Floppy drive interface cable not properly connected.	. Check cables and connectors for proper connection and correct orientation.

. Floppy disk drive failure.	. Check for proper jumper (if any) settings on floppy disk drive. . Check power (DC +5V, +12V) on floppy disk drive.
. DIP switch on main unit set wrongly, which indicates no floppy disk drive.	. Check for proper DIP switch settings on main unit.

Symptom

Floppy drive boot up normal. Unable to format or write data to drive, or fail to retrieve the data written by the same computer.

Possible causes	Solution
. Floppy drive failure.	. Check floppy drive.
. Floppy drive interface write logic failure.	. Check Gate Array C1 (U28), uPD765 (U27), U29.
. Floppy write data Precompensation failure.	. Check Gate Array C1 (U28), uPD765 (U27).
. Floppy drive signal cable broken.	. Check for proper connecting cable between card and disk drive.
. Diskette defective or improper media quality.	. Check diskette for double-sided, double-density and it is not defective.

Symptom

Transcopy function not working. Floppy disk function normal.

Possible causes	Solution
. Transcopy function not enabled.	. Check jumper block for proper setting.
. Address conflict with other I/O devices on the system slot.	. Check for I/O devices attached to system slot. Select another I/O address for Transcopy in case of conflict.
. Transcopy logic failure.	. Replace Gate Array C1 (U20).

5.3 PARALLEL PRINTER PORT FAILURE

Symptom

Printer Port not functioning properly.

Possible causes	Solution
. Printer cable and connectors not properly connected.	. Check for proper connection between the card and printer.
. Printer port not enabled (on newer versions of the card)	. Change jumper block setting to enable function.
. Operating System is assumming another parallel port, with different address, on another peripheral card.	. Check for another parallel port in the system. Use the other port for printer if higher priority is given to that port.
. Printer port logic failure.	. Check Gate Array C1 (U20), U2,U8,U3,U7.
. Printer interrupt failure.	. Check printer port interrupt logic in Gate Array C1 (U20), U9.

5.4 RS232C SERIAL INTERFACE PORT FAILURE

Symptom

RS232C Serial Interface Ports not functioning properly.

Possible causes	Solution
. Serial cables and connectors not connected properly.	. Check for proper connection between card and bracket, between connectors and serial device.
. Serial Ports not enabled (on newer versions of the card).	. Change jumper block settings to enable the function.
. Only one serial port is built-in on some cards.	. Expand to two serial ports. Refer to user's manual.
. Improper serial cable used for serial printer (different from modem cables).	. Check if the proper serial printer cable is used.
. Serial port hardware logic failure.	. Check Gate Array C1 (U20), ACE 8250 (U15, U16), RS232 signal convertors U10, U11,U17,U18,U19,U9, Xtal 1.

5.5 GAME PORT FAILURE

Symptom

Game Port not functioning properly.

Possible causes	Solution
. Joystick/paddle connector or cable not properly connected,	. Check for proper connection in the cable and connector of joystick/paddle.
. Defective joystick or paddle.	. Check for defective joystick/paddle device, or improper resistance value inside joystick.
. Game port hardware logic failure.	. Check Gate Array C1(U20),U5,U4,R1-R4,C26-C29.

5.6 REAL-TIME CLOCK FAILURE

Symptom

Real -Time Clock not responding, or lose time after power down, or no alarm.

Possible causes	Solution
. Real-time clock not enabled.	. Check for proper jumper setting to enable the function.
. Defective real-time clock hardware logic.	. Check Gate Array C1(U20),U23(or U22), Xtal 3, VC1, C84,Q1,Q2,D1,D2 U21,U26.
. Defective battery or charging circuit.	. Check 3.6V battery, C83,R17,D3.
. Computer or card not used for too long a time, resulting in battery exhausted.	. Power up the computer a few hours to charge the battery.
. Address conflict with other devices in the system.	. Check for address conflict and change to another address for the real-time clock.

Z765A FDC
Floppy Disk Controller

Zilog

NEW 1985

Advance Information
Product
Specification

April 1985

FEATURES

Address Mark detection circuitry internal to the FDC simplifies the phase locked loop and read electronics. The track stepping rate, head load time, and head unload time are user-programmable.

Z765A features are:

- IBM-compatible format, Single and Double Density
- Multisector and multitrack transfer capability
- Data scan capability—scans a single sector or an entire cylinder comparing byte-for-byte host memory and disk data
- Drives up to 4 floppy-disk drives (FDD)
- Data transfers in DMA or non-DMA mode
- Parallel seek operations on up to four drives
- Compatible with most general-purpose microprocessors
- Single phase 8 MHz clock
- +5V Only
- 40-Pin Dual-In-Line (DIP) package

GENERAL DESCRIPTION

The Z765A is an LSI Floppy Disk Controller (FDC) chip which contains the circuitry and control functions for interfacing a processor to four floppy-disk drives. It supports IBM System 3740 Single Density format (FM) and IBM System 34 Double Density format (MFM) including double-sided recording. The Z765A provides control signals which simplify the design of an external phase locked loop and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a floppy-disk interface. (Figure 1).

Handshaking signals make DMA operation easily incorporated with the aid of an external DMA Controller chip, such as the Z80 DMA. The FDC operates in either the DMA or non-DMA mode. In the non-DMA mode the FDC generates interrupts to the processor every time a data byte is to be transferred. In the DMA mode, the processor need only load the command into the FDC and all data transfers occur under control of the FDC and DMA controllers.

The Z765A executes 15 commands; each command requires multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The commands are:

- READ DATA
- WRITE DATA
- WRITE DELETED DATA
- READ DELETED DATA
- READ TRACK
- READ ID
- FORMAT TRACK
- SCAN EQUAL
- SCAN HIGH OR EQUAL
- SCAN LOW OR EQUAL
- SEEK
- RECALIBRATE
- SENSE INTERRUPT STATUS
- SPECIFY
- SENSE DRIVE STATUS

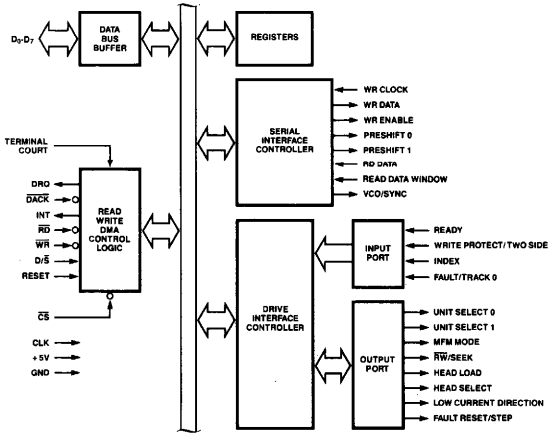


Figure 1. Z765A FDC Block Diagram

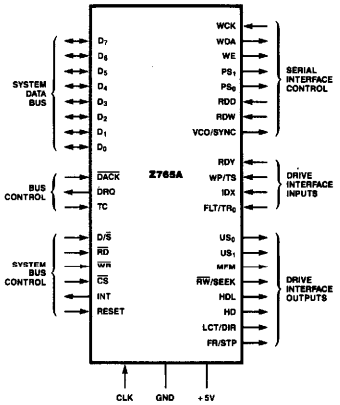


Figure 2. Pin Functions

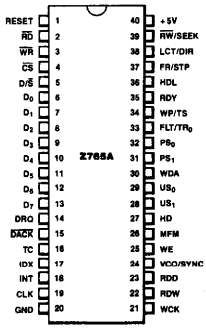


Figure 3. Pin Assignments

2357-001, 002, 003

PIN DESCRIPTIONS (Figures 2 and 3)

CLK. *Clock* (input). Single phase 8MHz square wave clock.

$\overline{CS}$. *Chip Select* (input). IC selected when 0 (Low), allowing $\overline{RD}$ and $\overline{WR}$ to be enabled.

D_0-D_7. *Data Bus.* Bidirectional 8-bit Data Bus. Disabled when $\overline{CS}$ = 1.

$\overline{DACK}$. *DMA Acknowledge* (input). DMA cycle is active when 0, and controller is performing DMA transfer.

DRQ. *Data DMA Request* (output). DMA Request is being made by FDC when DRQ = 1.

D/$\overline{S}$. *Data/Status Register Select* (input). Selects Data Register (D/$\overline{S}$ = 1) or Status Register (D/$\overline{S}$ = 0) contents of the FDC to be sent to Data Bus. Disabled when $\overline{CS}$ = 1.

FR/STP. *Fault Reset/Step* (output). Resets fault FF in FDD in Read/Write mode, contains step pulses to move head to another cylinder in Seek mode.

FLT/TR_0. *Fault/Track 0* (input). Senses FDD fault condition in Read/Write mode and Track 0 condition in Seek mode.

HD. *Head Select* (output). Head 1 selected when 1 (High); Head 0 selected when 0 (Low).

HDL. *Head Load* (output). Command which causes read/write head in FDD to contact diskette.

IDX. *Index* (input). Indicates the beginning of a disk track.

INT. *Interrupt* (output). Interrupt Request generated by FDC.

LCT/DIR. *Low Current/Direction* (output). Lowers Write current on inner tracks in Read/Write mode; determines direction head will step in Seek mode. A fault reset pulse is issued at the beginning of each Read or Write command prior to the occurrence of the Head Load signal.

MFM. *MFM Mode* (output). MFM mode when 1; FM mode when 0.

PS_1, PS_0. *Precompensation (preshift)* (output). Write precompensation status during MFM mode. Determines early, late, and normal times.

$\overline{RD}$. *Read* (input). When 0, control signal for transfer of data from FDC to Data Bus. Disabled when $\overline{CS}$ = 1.

RDD. *Read Data* (input). Read data from FDD, containing clock and data bits.

RDW. *Read Data Window* (input). Generated by PLL, and used to sample data from FDD.

RDY. *Ready* (input). Indicates FDD is ready to send or receive data.

RESET. *Reset* (input). Places FDC in idle state. Resets output lines to FDD to 0. Does not affect SRT, HUT or HLT in Specify command. If RDY pin is held High during Reset, FDC generates an interrupt within 1.024 msec. To clear this interrupt use Sense Interrupt Status command.

$\overline{RW}$/SEEK. *Read Write/Seek* (output). When 1 (High) Seek mode selected; when 0 (Low) Read/Write mode selected.

TC. *Terminal Count* (input). Indicates the termination of a DMA transfer when 1 (High). It terminates data transfer during Read/Write/Scan command in DMA or Interrupt mode.

US_1, US_0. *Unit Select* (output). FDD Unit selected.

VCO/SYNC. (output). Inhibits VCO in PLL when 0 (Low); enables VCO when 1.

WCK. *Write Clock* (input). Write data rate to FDD. FM = 500 KHz, MFM = 1 MHz with a pulse width of 250 ns for both FM and MFM.

WDA. *Write Data* (output). Serial clock and data bits to FDD.

WE. *Write Enable* (output). Enables write data into FDD.

WP/TS. *Write Protect/Two Side* (input). Senses Write Protect status in Read/Write mode and Two-Side Media in Seek mode.

$\overline{WR}$. *Write* (input). When 0, control signal for transfer of data to FDC via Data Bus. Disabled when $\overline{CS}$ = 1.

Table 1. Internal Registers

The bits in the Main Status Register are defined as follows:

Bit No.	Name	Symbol	Description
D_0	FDD 0 Busy	D_0B	FDD number 0 is in the Seek mode. If any bit is set, FDC will not accept read or write command.
D_1	FDD 1 Busy	D_1B	FDD number 1 is in the Seek mode. If any bit is set, FDC will not accept read or write command.
D_2	FDD 2 Busy	D_2B	FDD number 2 is in the Seek mode. If any bit is set, FDC will not accept read or write command.
D_3	FDD 3 Busy	D_3B	FDD number 3 is in the Seek mode. If any bit is set, FDC will not accept read or write command.
D_4	FDC Busy	CB	A read or write command is in process. FDC will not accept any other command.
D_5	Execution Mode	EXM	This bit is set only during execution phase in non-DMA mode. When D_5 goes low, execution phase has ended and result phase has started. It operates only during non-DMA mode of operation.
D_6	Data Input/Output	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO = 1, then transfer is from Data Register to the processor. If DIO = 0, transfer is from the processor to Data Register.
D_7	Request for Master	RQM	Indicates Data Register is ready to send or receive data to or from the processor. Both bits DIO and RQM should be used to perform the handshaking functions of "ready" and "direction" to the processor.

INTERNAL REGISTERS

The Z765A contains two registers which may be accessed by the main system processor: a Status register and a Data register. The 8-bit Main Status register (Table 1) contains the FDC status information and may be accessed at any time. The 8-bit Data register is several registers in a stack; one register at a time is presented to the data bus. The Data register stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data register in order to program or obtain the results after a particular command. Only the Status register may be read and used to facilitate the transfer of data between the processor and Z765A.

The relationship between the Status/Data registers and the signals $\overline{RD}$, $\overline{WR}$, and D/$\overline{S}$ is shown in Table 2.

The Data Input/Output (DIO) and Request for Master (RQM) bits in the Status register indicate when data is ready and the direction transfer on the data bus (Figure 4). The maximum time between the last $\overline{RD}$ or $\overline{WR}$ during a command or result phase and the set or reset DIO and RQM is 12μs; every time the Main Status register is read the CPU should wait 12μs. The maximum time from the trailing edge of the last $\overline{RD}$ in the result phase to when D_4 (FDC busy) goes Low is 12μs.

Table 2. Relationships Between Status/Data Registers and $\overline{RD}$, $\overline{WR}$, and D/$\overline{S}$

D/$\overline{S}$	$\overline{RD}$	$\overline{WR}$	Function
0	0	1	Read Main Status Register
0	1	0	Illegal
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register

STATUS REGISTER IDENTIFICATION

Bit No.	Name	Symbol	Description
			Status Register 0
D_7	Interrupt Code	IC	D_7 = 0 and D_6 = 0 Normal Termination of command, (NT). Command was completed and properly executed.
			D_7 = 0 and D_6 = 1 Abnormal Termination of command, (AT). Execution of command was started but was not successfully completed.
D_6			D_7 = 1 and D_6 = 0 Invalid Command issue, (IC). Command which was issued was never started.
			D_7 = 1 and D_6 = 1 Abnormal Termination because during command execution the ready signal from FDD changed state.
D_5	Seek End	SE	When the FDC completes the SEEK command, this flag is set to 1 (High).
D_4	Equipment Check	EC	If a fault signal is received from the FDD, or if the Track 0 signal fails to occur after 77 step pulses (Recalibrate Command) then this flag is set.
D_3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single-sided drive, then this flag is set.
D_2	Head Address	HD	This flag is used to indicate the state of the head at Interrupt.
D_1	Unit Select 1	US_1	This flag is used to indicate a Drive Unit Number at Interrupt.
D_0	Unit Select 0	US_0	This flag is used to indicate a Drive Unit Number at Interrupt.
			Status Register 1
D_7	End of Cylinder	EN	When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set.
D_6			Not used. This bit is always 0 (Low).
D_5	Data Error	DE	When the FDC detects a Cyclic Redundancy Check (CRC) error in either the ID field or the data field, this flag is set.
D_4	Overrun	OR	If the FDC is not serviced by the host system during data transfers within a certain time interval, this flag is set.
D_3			Not used. This bit always 0 (Low).
D_2	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or SCAN command, if the FDC cannot find the sector specified in the Internal Data Register (IDR), this flag is set.
			During execution of the READ ID command, if the FDC cannot read the ID field without an error, then this flag is set.
			During execution of the READ A cylinder command, if the starting sector cannot be found, then this flag is set.

STATUS REGISTER IDENTIFICATION (Continued)

Bit No.	Name	Symbol	Description
			Status Register 1 (Continued)
D_1	Not Writeable	NW	During execution of WRITE DATA, WRITE DELETED DATA or Format A cylinder command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set. If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in data field) of Status register 2 is set.
			Status Register 2
D_7			Not used. This bit is always 0 (Low).
D_6	Control Mark	CM	During execution of the READ DATA or SCAN command, if the FDC encounters a sector which contains a Deleted Data Address Mark, this flag is set.
D_5	Data Error in Data Field	DD	If the FDC detects a CRC error in the data field then this flag is set.
D_4	Wrong Cylinder	WC	This bit is related to the ND bit, and when the contents of Cylinder (C) on the medium is different from that stored in IDR, this flag is set.
D_3	Scan Equal Hit	SH	During execution of the SCAN command, if the condition of "equal" is satisfied, this flag is set.
D_2	Scan Not Satisfied	SN	During execution of the SCAN command, if the FDC cannot find a sector on the cylinder which meets the condition, then this flag is set.
D_1	Bad Cylinder	BC	This bit is related to the ND bit, and when the contents of C on the medium is different from that stored in the IDR and the contents of C is FF_H, then this flag is set.
D_0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.
			Status Register 3
D_7	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D_6	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D_5	Ready	RY	This bit is used to indicate the status of the Ready signal from the FDD.
D_4	Track 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
D_3	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
D_2	Head Address	HD	This bit is used to indicate the status of the Side Select signal to the FDD.
D_1	Unit Select 1	US_1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D_0	Unit Select 0	US_0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

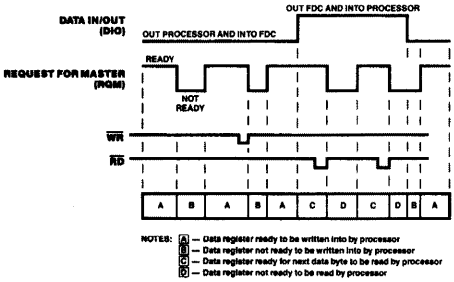


Figure 4. Data Transfer

COMMAND SEQUENCE

The Z765A is capable of performing 15 different commands. Each command is initiated by a multibyte transfer from the processor; the result after execution of the command may also be a multibyte transfer back to the processor. Because of this multibyte interchange of information between the Z765A and the processor, each command consists of three phases:

Command Phase. The FDC receives all information required to perform a particular operation form the processor.

Execution Phase. The FDC performs the operation it was instructed to do.

Result Phase. After completion of the operation, status and other housekeeping information are made available to the processor.

The Instruction set shows the required preset parameters and results for each command. Most commands require 9 command bytes and return 7 bytes during the result phase. The W to the left of each byte indicates a command phase byte to be written; an R indicates a result byte.

PROCESSOR INTERFACE

During Command or Result phases the Main Status register must be read by the processor before each byte of information is written into, or read from, the Data register. Then the CPU should wait for 12μs before reading the Main Status register. Bits D_6 and D_7 in the Main Status register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the Z765A. Many of the commands require multiple bytes and, as a result, the Main Status register must be read prior to each byte transfer to the Z765A. During the Result phase, D_6 and D_7 in the Main Status register must both be 1's before reading each byte from the Data Register. Reading the Main Status register before each byte transfer to the Z765A is required only in the Command and Result phases, not during the Execution phase.

If the Z765A is in the non-DMA mode and reading data from FDD, then the receipt of each data byte is indicated by an interrupt signal on pin 18(INT = 1). The generation of a Read signal ($\overline{RD}$ = 0) or Write signal ($\overline{WR}$ = 0) will clear the interrupt and output the data onto the data bus. If the processor cannot handle interrupts fast enough (every 13μs for the MFM mode and 27μs for the FM mode), then it may poll the Main Status register and bit D_7 (RQM) functions as the interrupt signal. If a Write command is in process, the $\overline{WR}$ signal negates the reset to the interrupt signal.

In the non-DMA mode it is necessary to examine the Main Status register to determine the cause of the interrupt, since it could be a data interrupt or a command termination interrupt, either normal or abnormal. If the Z765A is in the

COMMAND SYMBOL DESCRIPTION

Symbol	Name	Description
D/$\overline{S}$	Data/Status Select	D/$\overline{S}$ controls selection of Main Status register (D/$\overline{S}$ = 0) or Data register (D/$\overline{S}$ = 1)
C	Cylinder Number	C stands for the current/selected cylinder (track) numbers 0 through 76 of the medium.
D	Data	D stands for the data pattern which is going to be written into a sector.
D_7-D_0	Data Bus	8-bit Data Bus, where D_7 stands for a most significant bit, and D_0 stands for a least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the sector.
EOT	End of Track	EOT stands for the final sector number on a cylinder. During Read or Write operations, FDC will stop data transfer after a sector number equal to EOT.
GPL	Gap Length	GPL stands for the length of Gap 3. During Read/Write commands this value determines the number of bytes that VCO/SYNC will stay low after two CRC bytes. During Format command it determines the size of Gap 3.
H	Head Address	H stands for head number 0 or 1, as specified in ID field.
HD	Head	HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words.)
HLT	Head Load Time	HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	HUT stands for the head unload time after a Read or Write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	If MF is Low, FM mode is selected, and if it is High. MFM mode is selected.
MT	Multitrack	If MT is high, a Multitrack operation is performed. If MT = 1 after finishing Read/Write operation on side 0, FDC automatically starts searching for sector 1 on side 1.
N	Number	N stands for the Number of data bytes written in a sector.
NCN	New Cylinder Number	NCN stands for a New Cylinder Number or desired position of head which is going to be reached as a result of the Seek operation.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA mode.
PCN	Present Cylinder Number	PCN stands for the cylinder number or present position of Head at the completion of Sense Interrupt Status command.
R	Record	R stands for the sector number which will be read or written.
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data Address mark.
SRT	Step Rate Time	SRT stands for the Stepping Rate for the FDD (1 to 16 ms in 1 ms increments). Stepping Rate applies to all drives ($F_{(16)}$ = 1 ms, $E_{(16)}$ = 2 ms, $D_{(16)}$ = 3 ms, . . .).
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	ST0-3 stands for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by D/$\overline{S}$ = 0). ST0-3 may be read only after a command has been executed and contains information relevant to that particular command.
STP	Step	During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); if STP = 2, then alternate sectors are read and compared.
US_0, US_1	Unit Select	Used to select between drives 0-3.

INSTRUCTION SET[1, 2]

Phase	R/W	Data Bus D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Read Data										
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	See Note 3
	W	C								Sector ID information prior to
	W	H								command execution. The 4 bytes
	W	R								are commanded against header
	W	N								on Floppy disk.
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system
Result	R	ST0								Status information after command
	R	ST1								execution
	R	ST2								
	R	C								Sector ID information after
	R	H								command execution
	R	R								
	R	N								
Read Deleted Data										
Command	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	C								Sector ID information prior to
	W	H								command execution. The 4 bytes
	W	R								are commanded against header
	W	N								on Floppy Disk.
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system
Result	R	ST0								Status information after command
	R	ST1								execution
	R	ST2								
	R	C								Sector ID information after
	R	H								command execution
	R	R								
	R	N								

NOTES: 1. Symbols used in this table are described at the end of this section.
2. D/$\overline{S}$ should equal binary 1 for all operations.
3. X = Don't care, usually made to equal binary 0.

INSTRUCTION SET[1, 2] (Continued)

Phase	R/W	Data Bus D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Write Data										
Command	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	C								Sector ID information prior to command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the main system and FDD
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution.
	R	H								
	R	R								
	R	N								
Write Deleted Data										
Command	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	C								Sector ID information prior to command execution. The 4 bytes are commanded against header on Floppy disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

NOTES: 1. Symbols used in this table are described at the end of this section.
2. $D/\overline{S}$ should equal binary 1 for all operations.
3. X = Don't care, usually made to equal binary 0.

INSTRUCTION SET[1, 2] (Continued)

Phase	R/W	Data Bus D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Read A Track										
Command	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	C								Sector ID information prior to command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system. FDC reads all data fields from index hole to EOT.
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								
Read ID										
Command	W	0	MF	0	0	1	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
Execution										The first correct ID information on the cylinder is stored in Data Register.
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information read during Execution phase from Floppy Disk.
	R	H								
	R	R								
	R	N								

NOTES: 1. Symbols used in this table are described at the end of this section.
2. $D/\overline{S}$ should equal binary 1 for all operations.
3. X = Don't care, usually made to equal binary 0.

INSTRUCTION SET[1, 2] (Continued)

Phase	R/W	Data Bus D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Format A Track										
Command	W	0	MF	0	0	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	N								Bytes Sector
	W	SC								Sectors/Track
	W	GPL								Gap 3
	W	D								Filler byte
Execution										FDC formats an entire track.
Result	R	ST0								Status information after command
	R	ST1								execution
	R	ST2								
	R	C								In this case, the ID information
	R	H								has no meaning.
	R	R								
	R	N								
Scan Equal										
Command	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	C								Sector ID information prior to
	W	H								command execution
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data compared between the FDD and the main system.
Result	R	ST0								Status information after command
	R	ST1								execution
	R	ST2								
	R	C								Sector ID information after
	R	H								command execution
	R	R								
	R	N								

NOTES: 1. Symbols used in this table are described at the end of this section.
2. $D/\overline{S}$ should equal binary 1 for all operations.
3. X = Don't care, usually made to equal binary 0.

INSTRUCTION SET[1, 2] (Continued)

Phase	R/W	Data Bus D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Scan Low or Equal										
Command	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	C								Sector ID information prior to
	W	H								command execution
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data compared between the FDD and main system
Result	R	ST0								Status information after command
	R	ST1								execution
	R	ST2								
	R	C								Sector ID information after
	R	H								command execution
	R	R								
	R	N								
Scan High or Equal										
Command	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	C								Sector ID information prior to
	W	H								command execution.
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data compared between the FDD and main system.
Result	R	ST0								Status information after command
	R	ST1								execution
	R	ST2								
	R	C								Sector ID information after
	R	H								command execution.
	R	R								
	R	N								
Recalibrate										
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	X	X	X	X	X	0	US_1	US_0	
Execution										Head retracted to Track 0

NOTES: 1. Symbols used in this table are described at the end of this section.
2. $\overline{DS}$ should equal binary 1 for all operations.
3. X = Don't care, usually made to equal binary 0.

INSTRUCTION SET[1, 2] (Continued)

Phase	R/W	Data Bus D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Sense Interrupt Status										
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	ST0								Status information about the FDC
	R	PCN								at the end of seek operation
Specify										
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	SRT							HUT	
	W	HLT							ND	
Sense Drive Status										
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	X	X	X	X	X	0	US_1	US_0	
Result	R	ST3								Status information about FDD
Seek										
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	NCN								
Execution										Head is positioned over proper cylinder on diskette.
Invalid										
Command	W	Invalid Codes								Invalid Command Codes (NoOp—FDC goes into Standby state.)
Result	R	ST0								ST0 = $80_{(H)}$

NOTES: 1. Symbols used in this table are described at the end of this section.
2. $D/\overline{S}$ should equal binary 1 for all operations.
3. X = Don't care, usually made to equal binary 0.

DMA mode, no interrupts are generated during the Execution phase. The Z765A generates DRQs (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both a $\overline{DACK}$ (DMA Acknowledge) = 0 and an $\overline{RD}$ (Read signal) = 0. When the DMA Acknowledge signal goes Low ($\overline{DACK}$ = 0), then the DMA request is cleared (DRQ = 0). If a Write command has been issued, a $\overline{WR}$ signal appears instead of $\overline{RD}$. After the Execution phase has been completed [Terminal Count (TC) has occurred] or the last sector on the cylinder (EOT) read/written, then an interrupt occurs (INT = 1) which signifies the beginning of the Result phase. When the first byte of data is read during the Result phase, the interrupt is automatically cleared (INT = 0).

The $\overline{RD}$ or $\overline{WR}$ signals should be asserted while $\overline{DACK}$ is true. The $\overline{CS}$ signal is used in conjunction with $\overline{RD}$ and $\overline{WR}$ as a gating function during programmed I/O operations. $\overline{CS}$ has no effect during DMA operations. If the non-DMA mode is chosen, the $\overline{DACK}$ signal should be pulled up to V_{CC}.

During the Result phase all bytes shown in the Command Table must be read. For example, the Read Data command has seven bytes of data in the Result phase; all seven bytes must be read to successfully complete the Read Data command and allow the Z765A to accept a new command.

The Z765A contains five Status registers. The Main Status register can be read at any time by the processor. The other four Status registers (ST0, ST1, ST2, and ST3) are available only during the Result phase and can be read only after completing a command. The particular command that has been executed determines how many of the Status registers are read.

The bytes of data which are sent to the Z765A to form the Command phase and are read out of the Z765A in the Result phase must occur in the order shown in the Command Table. That is, the Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result phases is allowed. After the last byte of data in the Command phase is sent to the Z765A, the Execution phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result phase, the command is automatically ended and the Z765A is ready for a new command.

POLLING FEATURE OF THE Z765A

After Reset is sent to the Z765A, the Unit Select lines US_0 and US_1 automatically go into a polling mode (Figure 5). Between commands (and between step pulses in the Seek command) the Z765A polls all four FDDs looking for a change in the Ready line from any of the drives. If the Ready line changes state (usually due to a door opening or closing), then the Z765A generates an interrupt. When Status register 0 (ST0) is read (after Sense Interrupt Status is issued), Not Ready (NR) is indicated. The polling of the Ready line by the Z765A occurs continuously between commands, thus notifying the processor which drives are on or off line. Each drive is polled every 1.024 ms except during the Read/Write commands. When used with a 4 MHz clock for interfacing to minifloppies, the polling rate is 2.048 ms.

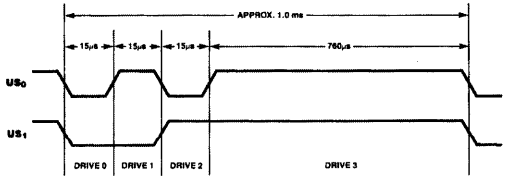


Figure 5. Polling Features

COMMANDS

Read Data

A set of nine (9) byte words are required to place the FDC into the Read Data Mode. After the Read Data command is issued, the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID Address Marks and ID fields. When the current sector number (R) stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC, via the data bus, outputs data byte-to-byte from the data field to the main system.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a Multi-Sector Read Operation. The Read Data command can be terminated by the receipt of a TC signal which should be issued when the DACK for the last byte of data is sent. Upon receipt of this signal, the FDC stops outputting data to the processor, but continues to read data from the current sector, checks Cyclic Redundancy Count (CRC), and at the end of the sector, terminates the Read Data command. The amount of data which can be handled with a single command to the FDC depends upon multitrack (MT), MFM/FM (MF), and Number of Bytes/Sector (N). Table 3 shows the Transfer Capacity.

Table 3. Transfer Capacity

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskettes
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

MT allows the FDC to read data from both sides of the diskette. For a particular cylinder, data is transferred starting at Sector 1, Side 0 and completing at the last sector, Sector L, Side 1. This function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector is not sent to the Data Bus. The FDC internally reads the complete sector performing the CRC check and, depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to FF_H.

At the completion of the Read Data Command the head is unloaded, after the Head Unload Time Interval specified in the Specify Command has elapsed. If the processor issues another command before the head unloads, there is no head settling time between subsequent reads. This time saved is particularly valuable when a diskette is copied.

If the FDC twice detects the index hole without finding the right sector (R), then the FDC sets Status register 1's No Data (ND) flag to 1, and terminates the Read Data command. (Status register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data fields in each sector, the FDC checks the CRC bytes. If a read error is detected indicating incorrect CRC in the ID field, the FDC sets Status register 1's Data Error (DE) flag to 1, and if a CRC error occurs in the Data Field, the FDC also sets Status register 2's Data Error in Data Field (DD) flag to 1, and terminates the Read Data command. (Status register 0, bit 7 = 0, bit 6 = 1.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit D in the first Command Word = 0, then the FDC sets Status register 2's Control Mark (CM) flag to 1, and after reading all the data in the sector, terminates the Read Data command. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector. When SK = 1, the CRC bits in the deleted data field are not checked.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27μs in the FM Mode, and every 13μs in the MFM Mode, or the FDC sets Status register 1's Overrun (OR) flag to 1, and terminates the Read Data command.

If the processor terminates a read or write operation in the FDC, then the ID information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 4 shows the values for C, H, R, and N when the processor terminates the command.

Table 4. C, H, R, and N Values When Processor Terminates Commands

MT	HD	Final Sector Transferred to Processor	ID Information at Result Phase			
			C	H	R	N
0	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	C + 1	NC	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	C + 1	NC	R = 01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	NC	LSB	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	C + 1	LSB	R = 01	NC

NOTES: NC (No Change): The same value as the one at the beginning of command execution.
LSB (Least Significant Bit): The least significant bit of H is complemented.

Write Data

A set of nine (9) bytes is required to set the FDC in the Write Data mode. After the Write Data command is issued, the FDC loads the head, waits the specified head setting time, and begins reading ID fields. When all four bytes (C, H, R, and N) loaded during the command match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus and outputs it to the FDD.

After writing data into the current sector, the sector number stored in the R register is incremented by one, and new data is written into the next data field. The FDC continues this Multisector Write Operation until a Terminal Count signal is issued. If a Terminal Count signal is sent to the FDC, it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written, the remainder of the data field is filled with zeros.

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (CRC error) in one of the ID fields, it sets Status register 1's DE flag to 1, and terminates the Write Data command. (Status register 0, bit 7 = 0, bit 6 = 1.)

The Write command operates in the same manner as the Read command for the following items:

- Transfer capacity
- End of cylinder (EN) flag
- No data (ND) flag
- Head unload time interval
- ID information when the processor terminates command
- Definition of DTL when N = 0 and when N ≠ 0

Refer to the Read Data command for details.

In the Write Data mode, data transfers between the processor and FDC via the data bus, must occur every 27μs in the FM mode and every 13μs in the MFM mode. If the time interval between data transfers is longer, then the FDC sets Status register 1's Overrun (OR) flag to 1, and terminates the Write Data command. (Status register 0, bit 7 = 0, bit 6 = 1.)

Write Deleted Data

This command is the same as the Write Data command except a Deleted Data Address mark, instead of the normal Data Address mark, is written at the beginning of the data field.

Read Deleted Data

This command is the same as the Read Data command except that when the FDC detects a Data Address mark at the beginning of a data field and SK = 0, the FDC reads all the data in the sector and sets Status register 2's CM flag to 1, and terminates the command. If SK = 1, then the FDC skips the sector with the Data Address mark and reads the next sector.

Read Track

This command is similar to the Read Data command except that this is a continuous Read operation where the entire data field from each of the sectors is read. Immediately after

sensing the index hole, the FDC starts reading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID or Data CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR and, if there is no comparison, sets Status register 1's ND flag to 1. Multitrack or skip operations are not allowed with this command.

This command terminates when the number of sectors read is equal to EOT. If the FDC does not find an ID Address mark on the diskette after it senses the index hole for the second time, it sets Status register 1's Missing Address mark (MA) flag to 1 and terminates the command. (Status Register 0, bit 7 = 0, bit 6 = 1.)

Read ID

The Read ID command gives the present position of the recording head. The FDC stores the values from the first ID field it can read. If no proper ID Address mark is found on the diskette before the index hole is encountered for the second time, Status register 1's MA flag is set to 1; if no data is found, Status register 1's No Data (ND) flag is set to 1. The command is then terminated with STO bit 7 = 0 and bit 6 = 1. During this command, data transfer between FDC and the CPU occurs only during the result phase.

Format Track

The Format command allows an entire track to be formatted. After the index hole is detected, data is written on the diskette; Gaps, Address marks, ID fields and data fields, all per the IBM 3740 Single Density format or IBM System 34 Double Density format, are recorded. The processor, during the command phase, supplies values i.e., Number of bytes/sector (N), Sectors Cylinder (SC), Gap Length (GPL), and Data Pattern (D) which determine the particular format to be written.

The data field is filled with the byte of data stored in D. The ID field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for Cylinder number (C), Head number (H), Sector number (R), and Number of bytes/sector (N). This allows diskette formatting with nonsequential sector numbers.

The processor must send new values for C, H, R, and N to the Z765A for each sector on the track. If FDC is set for the DMA mode, it issues four DMA requests per sector. If it is set for the Interrupt mode, it issues four interrupts per sector and the processor must supply C, H, R, and N loads for each sector. The contents of the R register are incremented by 1 after each sector is formatted; thus, the R register contains a value of R when it is read during the Result phase. This incrementing and formatting continues for the whole track until the FDC detects the index hole for the second time, whereupon it terminates the command.

If the Fault signal is received from the FDD at the end of a Write operation, the FDC sets Status register 0's EC flag to 1 and terminates the command after setting Status register 0, bit 7 to 0 and bit 6 to 1. Also the loss of a Ready signal at the beginning of a command execution phase causes Status register 0, bit 7 and 6 to be set to 0 and 1 respectively.

Table 5 shows the sector size relationship between N, SC, and GPL.

Table 5. Functional Description of Commands

Format	Sector Size	N	SC	GPL[1]	GPL[2,3]
8" Standard Floppy					
FM Mode	128 bytes sector	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM Mode[4]	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
5¼" Minifloppy					
FM Mode	128 bytes/sector	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM Mode[4]	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF

NOTES:
1. Suggested values of GPL in Read or Write commands to avoid splice point between data field and ID field of contiguous sections.
2. Suggested values of GPL in format command.
3. All values except sector size are hexidecimal.
4. In MFM mode FDC cannot perform a Read/Write format operation with 128 bytes sector (N = 00)

Scan Commands

The Scan commands allow comparison of data read from the diskette and data supplied from the main system. The FDC compares the data on a byte-by-byte basis and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} \leq D_{Processor}$, or $D_{FDD} \geq D_{Processor}$. The hexadecimal byte of FF from memory or from FDD can be used as a mask byte because it always meets the condition of the comparison. One's complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP → R) and the scan operation continues until one of the following conditions occur: the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count (TC) signal is received.

If the conditions for scan are met, the FDC sets the Status register 2's Scan Hit (SH) flag to 1 and terminates the Scan command. If the conditions for scan are not met between the starting sector number (R) and the last sector on the cylinder (EOT), then the FDC sets Status register 2's Scan Not Satisfied (SN) flag to 1, and terminates the Scan command. During the scan operation, the receipt of a signal from the processor or DMA controller causes the FDC to complete the comparison of the particular byte in process and then to terminate the command. Table 6 shows the status of bits SH and SN under various conditions of Scan.

Table 6.

Command	Status Register 2		Comments
	Bit 2 = SN	Bit 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan Low or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} > D_{Processor}$
Scan High or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} > D_{Processor}$
	1	0	$D_{FDD} < D_{Processor}$

If the FDC encounters a Deleted Data Address mark on one of the sectors and SK = 0, then it regards the sector as the last sector on the cylinder, sets Status register 2's Control Mark (CM) flag to 1 and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address mark, reads the next sector, and sets Status register 2's Control Mark (CM) flag to 1 to show that a Deleted sector has been encountered.

When either the Step (STP) (contiguous sectors = 01 or alternate sectors = 02) sectors are read or the Multitrack (MT) is programmed, the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26 and the Scan command is started at sector 21, the following happens. Sectors 21, 23, and 25 are read, then the next sector, 26, is skipped and the index hole is encountered before the EOT value of 26 can be read resulting in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan command would be completed in a normal manner.

During the Scan command, data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having Status register 1's Overrun (OR) flag set, it is necessary to have the data available in less than 27μs (FM mode) or 13μs (MFM mode). If an Overrun occurs, the FDC ends the command with Status register 0, bit 7 cleared to 0 and bit 6 set to 1.

Seek

The Read/Write head within the FDD is moved from cylinder to cylinder under control of the Seek command. The FDC has four independent Present Cylinder registers for each drive which are cleared only after the Recalibrate command. The FDC compares the Present Cylinder Number (PCN) which is the current head position with the New Cylinder Number (NCN), and if there is a difference, performs the following operations:

PCN < NCN: Direction signal to FDD set to 1, and Step Pulses are issued. (Step In)

PCN > NCN: Direction signal to FDD cleared to 0, and Step Pulses are issued. (Step Out)

The rate at which Step pulses are issued is controlled by Stepping Rate Time (SRT) in the Specify command. After each Step pulse is issued NCN is compared against PCN, and when NCN = PCN, Status register 0's Seek End (SE) flag is set to 1, and the command is terminated. At this point FDC interrupt goes High. Bits D_0-D_3 in the Main Status register are set during the Seek operation and are cleared by the Sense Interrupt Status command.

During the command phase of the Seek operation the FDC is in the FDC Busy state, but during the execution phase it is in the Nonbusy state. While the FDC is in the Nonbusy state, another Seek command may be issued, and in this manner parallel Seek operations may be done on up to four drives at once. No other command can be issued for as long as the FDC is in the process of sending step pulses to any drive.

If an FDD is in a Not Ready state at the beginning of the command execution phase or during the Seek operation, then Status register 0's Not Ready (NR) flag is set to 1, and the command is terminated after bit 7 is set to 1 and bit 6 to 0.

If writing three bytes of Seek command exceeds 150μs, the timing between the first two step pulses may be 1ms shorter than that set in the Specify command.

Recalibrate

The function of this command is to retract the Read/Write head within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is Low, the Direction signal remains 0 and step pulses are issued. When the Track 0 signal goes High, the Status register 0's SE flag is set to 1 and the command is terminated. If the Track 0 signal is still Low after 77 step pulses have been issued, the FDC sets Status register 0's SE and Equipment Check (EC) flags to 1s and terminates the command after Status register 0, bit 7 is cleared to 0 and bit 6 is set to 1.

The ability to do overlap Recalibrate commands to multiple FDDs and the loss of the Ready signal, as described in the Seek command, also applies to the Recalibrate command. If the Diskette has more than 77 tracks, the Recalibrate command should be issued twice, in order to position the Read/Write head to Track 0.

Sense Interrupt Status

An interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result phase of command:
   - □ Read Data
   - □ Write Data
   - □ Write Deleted Data
   - □ Read Deleted Data
   - □ Read Track
   - □ Read ID
   - □ Format Track
   - □ Scan
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate command
4. During Execution phase in the non-DMA mode

Interrupts caused by reasons 1 and 4 occur during normal command operations and are easily discernible by the processor. During an execution phase in non-DMA mode, D_5 in the Main Status Register is High. Upon entering the Result phase this bit is cleared. Reasons 1 and 4 do not require Sense Interrupt Status commands. The interrupt is cleared by Reading/Writing data to the FDC. Interrupts caused by reasons 2 and 3 may be uniquely identified with the aid of the Sense Interrupt Status command which resets the Interrupt signal and, via bits 5, 6, and 7 of Status register 0, identifies the cause of the interrupt (Table 7).

Table 7. Interrupt Identification

Seek End	Interrupt Code		
Bit 5	Bit 6	Bit 7	Cause
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate command
1	1	0	Abnormal Termination of Seek or Recalibrate command

The Sense Interrupt Status command is used in conjunction with the Seek and Recalibrate commands which have no result phase. When the disk has reached the desired head position, the Z765A sets the interrupt line true. The host CPU must then issue a Sense Interrupt Status command to determine the actual cause of the interrupt, which could be Seek End or a change in ready status from one of the drives. Figure 6 is a graphic example.

Specify

The Specify command sets the initial values for each of the three internal timers. The Head Unload Time (HUT) defines the time from the end of the execution phase of one of the Read/Write commands to the head unload state. This timer is programmable from 16 to 240ms in increments of 16ms (01 = 16ms, 02 = 32ms...OF_{16} = 240ms). The Step Rate Time (SRT) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16ms in increments of 1ms (F = 1ms, E = 2ms, and D = 3ms). The Head Load Time (HLT) defines the time between the Head Load signal's going High and the start of the Read/Write operation. This timer is programmable from 2 to 254ms in increments of 2ms (01 = 2ms, 02 = 4ms, 03 = 6ms...7F = 254ms).

The time intervals mentioned are a direct function of the 8MHz clock; if the clock were reduced to 4MHz (minifloppy application), all time intervals would be increased by a factor of 2.

The choice of a DMA or non-DMA operation is made by the Non-DMA (ND) bit. When this bit is High (ND = 1), the Non-DMA mode is selected; when ND = 0, the DMA mode is selected.

Sense Drive Status

The processor uses this command to obtain the status of the FDDs. Status register 3 contains the Drive Status information stored internally in FDC registers.

Invalid

If an Invalid command (not defined above) is sent to the FDC, then the FDC terminates the command after Status Register 0 bit 7 is set to 1 and bit 6 to 0. No interrupt is generated by the Z765A during this condition. Bits 6 and 7 (DIO and RQM) in the Main Status register are both High, indicating to the processor that the Z765A is in the Result phase and the contents of Status register 0 (STO) must be read. When the processor reads Status register 0, it finds an 80_H indicating the receipt of an Invalid command.

A Sense Interrupt Status command must be sent after a Seek or Recalibrate Interrupt, otherwise the FDC considers the next command as an Invalid command.

This command may be used as a No-Op command to place the FDC in a standby or No Operation state.

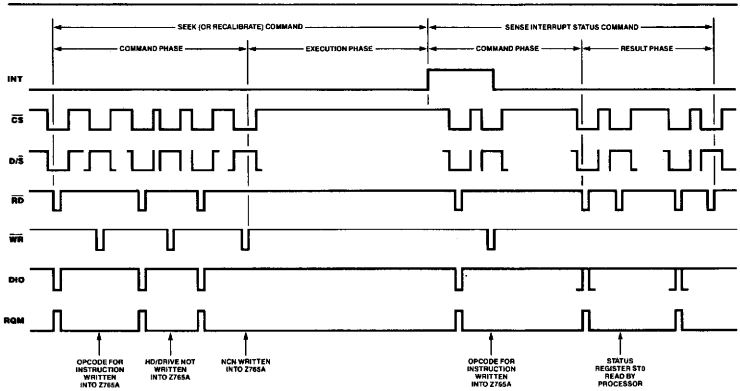


Figure 6. Seek, Recalibrate, and Sense Interrupt Status

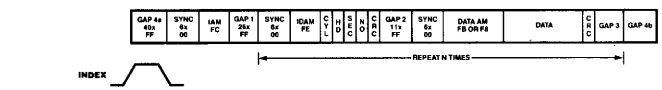


Figure 7. Data Format, FM Mode

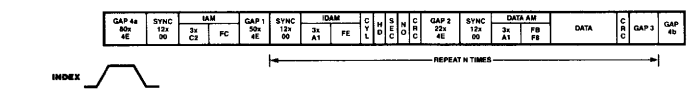


Figure 8. Data Format, MFM Mode

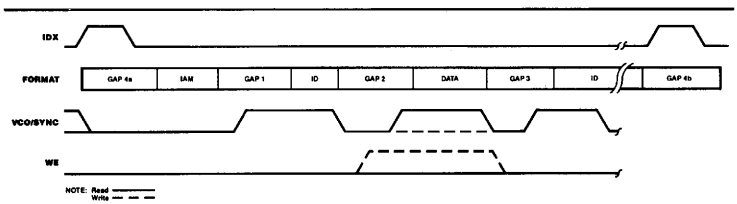


Figure 9. Data Timing Relationships

2357-006, 007, 008, 009

AC CHARACTERISTICS

T_A = −10°C to + 70°C; V_{CC} = +5V ± 5% unless otherwise specified.

Number	Symbol	Parameter	Min	Typ[1]	Max	Unit	Test Condition
			120	125	500	ns	
1	TcC	Clock Cycle Time		125		ns	8" FDD
				250		ns	5¼" FDD
2	TwCh	Clock Width (High)	40			ns	
3	TrC	Clock Rise Time			20	ns	
4	TfC	Clock Fall Time			20	ns	
5	TsAR	D/$\overline{S}$, $\overline{CS}$, $\overline{DACK}$ to $\overline{RD}$ ↓ Setup Time	0			ns	
6	ThRA	D/$\overline{S}$, $\overline{CS}$, $\overline{DACK}$ from $\overline{RD}$ ↑ Hold Time	0			ns	
7	TwRD	$\overline{RD}$ Width	250			ns	
8	TdRDf (Do)	$\overline{RD}$ ↓ to Data Output Delay			200	ns	C_L = 100 pf
9	TdRDr (Dz)	$\overline{RD}$ ↑ to Data Float Delay	20		100	ns	C_L = 100 pf
10	TsCS(WRf)	Control Signal (D/$\overline{S}$, $\overline{CS}$, $\overline{DACK}$) to $\overline{WR}$ ↓ Setup Time	0			ns	
11	ThCS(WRr)	Control Signal (D/$\overline{S}$, $\overline{CS}$, $\overline{DACK}$) from $\overline{WR}$ ↑ Hold Time	0			ns	
12	TwWR	$\overline{WR}$ Width	250			ns	
13	TsD(WRr)	Data to $\overline{WR}$ ↑ Setup Time	150			ns	
14	ThD(WRr)	Data from $\overline{WR}$ ↑ Hold Time	5			ns	
15	TdRDr(INT)	$\overline{RD}$ ↑ to INT Delay Time			500	ns	
16	TdWRr(INT)	$\overline{WR}$ ↑ to INT Delay Time			500	ns	
17	TcDRQ	DRQ Cycle Time	13			µs	
18	TdDRQ(DACK)	$\overline{DACK}$ ↓ to DRQ ↓ Delay			200	ns	
19	TdDACK(DRQ)	DRQ ↑ to $\overline{DACK}$ ↓ Delay	200			ns	TcC = 125 ns
20	TwDACK	$\overline{DACK}$ Width	2			TcC	
21	TwTC	TC Width	1			TcC	
22	TwRST	Reset Width	14			TcC	
				4		µs	MFM = 0 5¼"
23	TcWCK	WCK Cycle Time		2		µs	MFM = 1 5¼"
				2		µs	MFM = 0 8"
				1		µs	MFM = 1 8"
24	TwWCKh	WCK Width (High)	80	250	350	ns	
25	TrWCK	WCK Rise Time			20	ns	
26	TfWCK	WCK Fall Time			20	ns	
27	TdWCKr(PS)	WCK ↑ to Preshift Delay Time	20		100	ns	
28	TdWCKr(WEr)	WCK ↑ to WE ↑ Delay Time	20		100	ns	
29	TdWCKr(WDA)	WCK ↑ to WDA Delay Time	20		100	ns	
30	TwRDDh	RDD Width (High)	40			ns	
				4		µs	MFM = 0 5¼"
31	TWCY	Window Cycle Time		2		µs	MFM = 1 5¼"
				2		µs	MFM = 0 8"
				1		µs	MFM = 1 8"
32	TsW(RDDh) ThW(RDDl)	Window to RDD ↑ Setup Time Window from RDD ↓ Hold Time	15			ns	
33	TsUS(RWh)	Unit Select to $\overline{RW}$/SEEK ↑ Setup Time	12			µs	
34	TsRWr(DIR)	$\overline{RW}$/SEEK ↑ to LCT/DIR Setup Time	7			µs	
35	TsDIR(STEPr)	LCT/DIR to STEP ↑ Setup Time	1			µs	
36	ThUS(STEPl)	Unit Select from STEP ↓ Hold Time	5			µs	

NOTES: 1. Typical values for T_A = 25°C and nominal supply voltage.
2. Under software control, the range is from 1 ms to 16 ms at 8 MHz clock period.

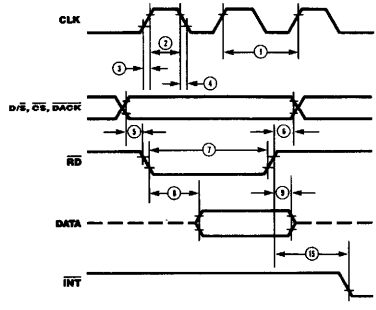
AC CHARACTERISTICS (Continued)

T_A = −10°C to + 70°C; V_{CC} = +5V ± 5% unless otherwise specified.

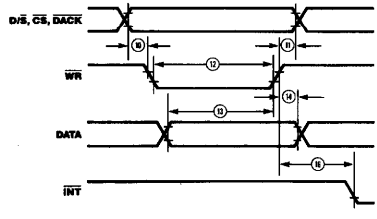
Number	Symbol	Parameter	Min	Typ[1]	Max	Unit	Test Condition
37	TwSTEPh	STEP Width (High)	6	7	8	µs	
38	TcSTEP	STEP Cycle Time	16	Note 2	Note 2	µs	
39	TwFRh	FAULT RESET Width (High)	8		10	µ	
40	TwWDAh	Write Data (WDA) Width (High)	T_D-50			ns	
41	ThUS(SEEKf)	Unit Select from $\overline{RW}$/SEEK ↓ Hold Time	15			µs	
42	ThSEEK(DIR)	$\overline{RW}$/SEEK from LCT/DIR Hold Time	30			µs	
43	ThDIR(STEPf)	LCT/DIR from STEP ↓ Hold Time	24			µs	
44	TwIDX	INDEX Width (High and Low)	10			TcC	
45	TdDRQh(RDI)	DRQ ↑ to $\overline{RD}$ ↓ Delay Time	800			µs	
46	TdDRQh(WRI)	DRQ ↑ to $\overline{WR}$ ↓ Delay Time	250			µs	
47	TdDRQh(RWh)	DRQ ↑ to $\overline{RD}$ ↑ or $\overline{WR}$ ↑ Delay Time			12	µs	

NOTES: 1. Typical values for T_A = 25°C and nominal supply voltage.
2. Under software control, the range is from 1 ms to 16 ms at 8 MHz clock period.

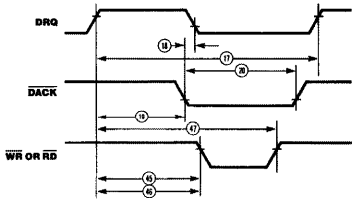
Processor Read Operation



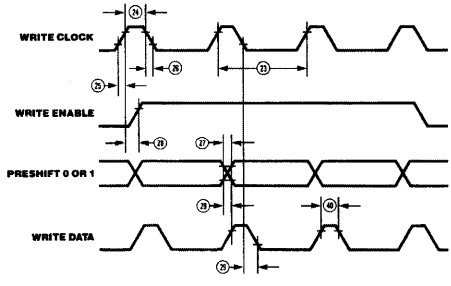
Processor Write Operation



DMA Operation

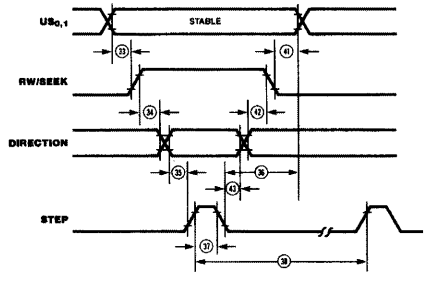


FDD Write Operation



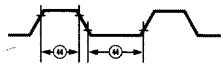
	Preshift 0	Preshift 1
Normal	0	0
Late	0	1
Early	1	0

Seek Operation

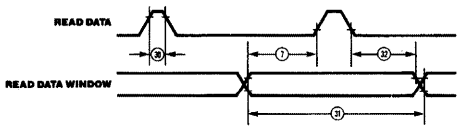


FLT Reset

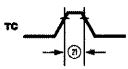
INDEX



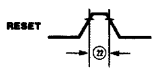
FDD Read Operation



Terminal Count



RESET



ABSOLUTE MAXIMUM RATINGS

T_A = 25°C

Operating Temperature . . . . . .0°C to + 70°C
Storage Temperature . . . . . – 65°C to + 150°C
All Output Voltages . . . . . – .3V to + 7V
All Input Voltages . . . . . – .3V to + 7V
Supply Voltage V_{CC} . . . . . – .3V to + 7V
Power Dissipation 1W

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above these indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_A = 0°C to + 70°C; V_{CC} = + 5V ± 5% unless otherwise specified.

Symbol	Parameter	Min	Typ*	Max	Unit	Test Condition
V_{IL}	Input Low Voltage	– 0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.40	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = – 200 μA
V_{ILC}	Input Low Voltage (CLK + WR Clock)	– 0.3		0.45	V	
V_{IHC}	Input High Voltage (CLK + WR Clock)	2.4		V_{CC} + 0.3	V	
I_{CC}	V_{CC} Supply Current			150	mA	
I_{LI}	Input Load Current (All Input Pins)			10	μA	V_{IN} = V_{CC}
				– 10	μA	V_{IN} = 0V
I_{LOH}	High Level Output Leakage Current			10	μA	V_{OUT} = V_{CC}
I_{LOL}	Low Level Output Leakage Current			– 10	μA	V_{OUT} = + 0.40V

*Typical values for T_A = 25°C and nominal supply voltage.

CAPACITANCE

T_A = 25°C; f_c = 1 MHz; V_{CC} = 0V

Symbol	Parameter	Min	Max	Unit	Test Condition
C_{CLOCK}	Clock Input Capacitance		20	pF	All pins except pin under
C_{IN}	Input Capacitance		10	pF	test tied to AC Ground
C_{OUT}	Output Capacitance		20	pF	

ORDERING INFORMATION

Ordering information is available from your local Zilog Sales Office.

Package drawings are in the Package Information section in this book.

Refer to the Literature List for additional documentation.

00-2357-01

National Semiconductor

Preliminary
May 1980

INS8250-B Asynchronous Communications Element

General Description

The INS8250 is a programmable Asynchronous Communications Element (ACE) chip contained in a standard 40-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate technology, functions as a serial data input/output interface in a microcomputer system. The functional configuration of the INS8250 is programmed by the system software via a TRI-STATE® 8-bit bidirectional data bus.

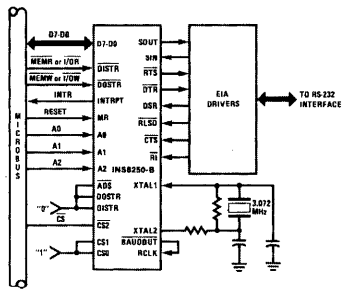
The INS8250 performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the INS8250 at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the INS8250, as well as any error conditions (parity, overrun, framing, or break interrupt).

In addition to providing control of asynchronous data communications, the INS8250 includes a programmable Baud Generator that is capable of dividing the timing reference clock input by divisors of 1 to $(2^{16} - 1)$, and producing a 16x clock for driving the internal transmitter logic. Provisions are also included to use this 16x clock to drive the receiver logic. Also included in the INS8250 is a complete MODEM-control capability, and a processor-interrupt system that may be software tailored to the user's requirements to minimize the computing time required to handle the communications link.

Features

- Designed to be Easily Interfaced to Most Popular Microprocessors.
- Adds or Deletes Standard Asynchronous Communication Bits (Start, Stop, and Parity) to or from Serial Data Stream
- Full Double Buffering Eliminates Need for Precise Synchronization
- Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts
- Programmable Baud Rate Generator Allows Division of Any Input Clock by 1 to $(2^{16} - 1)$ and Generates the Internal 16x Clock
- Independent Receiver Clock Input
- MODEM Control Functions (CTS, RTS, DSR, DTR, RI, and Carrier Detect)
- Fully Programmable Serial-Interface Characteristics
  - 5-, 6-, 7-, or 8-Bit Characters
  - Even, Odd, or No-Parity Bit Generation and Detection
  - 1-, 1½-, or 2-Stop Bit Generation
  - Baud Rate Generation (DC to 56k Baud)
- False Start Bit Detection
- Complete Status Reporting Capabilities
- TRI-STATE TTL Drive Capabilities for Bidirectional Data Bus and Control Bus
- Line Break Generation and Detection
- Internal Diagnostic Capabilities
  - Loopback Controls for Communications Link Fault Isolation
  - Break, Parity, Overrun, Framing Error Simulation
- Full Prioritized Interrupt System Controls
- Single +5-Volt Power Supply
- MICROBUS™* Compatible

INS8250-B MICROBUS Configuration



*Trademark, National Semiconductor Corp.

μPG-FL5M50/Printed in U.S.A.

Absolute Maximum Ratings

Temperature Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
All Input or Output Voltages with Respect to V_{SS} . . . . −0.5 V to +7.0 V
Power Dissipation . . . . . 400 mW

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.

DC Electrical Characteristics

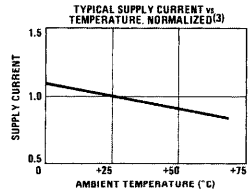
T_A = 0°C to +70°C, V_{CC} = +5 V ± 5%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{ILX}	Clock Input Low Voltage	−0.5		0.8	V	
V_{IHX}	Clock Input High Voltage	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	−0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 1.6 mA on all outputs,
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −100 μA
I_{CC} (AV)	Avg Power Supply Current (V_{CC})		65	80	mA	
I_{IL}	Input Leakage			±10	μA	
I_{CL}	Clock Leakage			±10	μA	

Capacitance

T_A = 25°C, V_{CC} = V_{SS} = 0 V

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
C_{XIN}	Clock Input Capacitance		15	20	pF	
C_{XOUT}	Clock Output Capacitance		20	30	pF	f_c = 1 MHz
C_{IN}	Input Capacitance		6	10	pF	Unmeasured pins returned to V_{SS}
C_{OUT}	Output Capacitance		10	20	pF	



AC Electrical Characteristics

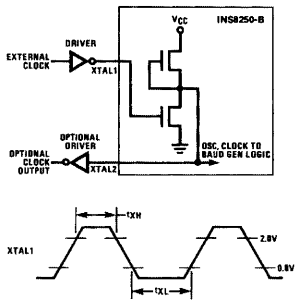
T_A = 0°C to ± 70°C, V_{CC} ± 5%

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{AW}	Address Strobe Width	120	—	ns	
t_{AS}	Address Setup Time	110	—	ns	
t_{AH}	Address Hold Time	60	—	ns	
t_{CS}	Chip Select Setup Time	110	—	ns	
t_{CH}	Chip Select Hold Time	60	—	ns	
t_{CSS}	Chip Select Output Delay from Strobe	0	100	ns	-@ 100pF loading
t_{DID}	$\overline{\text{DISTR}}$/DISTR Strobe Delay	0	—	ns	
t_{DIW}	$\overline{\text{DISTR}}$/DISTR Strobe Width	350	—	ns	
t_{RC}	Read Cycle Delay	1735	—	ns	
RC	Read Cycle = t_{AW} + t_{DID} + t_{DIW} + t_{RC}	2205	—	ns	
t_{DD}	$\overline{\text{DISTR}}$/DISTR to Driver Disable Delay	—	250	ns	-@ 100 pF loading
t_{DDD}	Delay from DISTR/$\overline{\text{DISTR}}$ to Data	—	300	ns	-@ 100 pF loading
t_{HZ}	$\overline{\text{DISTR}}$/DISTR to Floating Data Delay	100	—	ns	-@ 100 pF loading
t_{DOD}	$\overline{\text{DOSTR}}$/DOSTR Strobe Delay	50	—	ns	
t_{DOW}	$\overline{\text{DOSTR}}$/DOSTR Strobe Width	350	—	ns	
t_{WC}	Write Cycle Delay	1785	—	ns	
WC	Write Cycle = t_{AW} + t_{DOD} + t_{DOW} + t_{WC}	2305	—	ns	
t_{DS}	Data Setup Time	350	—	ns	
t_{DH}	Data Hold Time	100	—	ns	
t_{CSC}*	Chip Select Output Delay from Select	—	200	ns	-@ 100pF loading
t_{RA}*	Address Hold Time from $\overline{\text{DISTR}}$/DISTR	50	—	ns	
t_{RCS}*	Chip Select Hold Time from $\overline{\text{DISTR}}$/DISTR	50	—	ns	
t_{AR}*	$\overline{\text{DISTR}}$/DISTR Delay from Address	110	—	ns	
t_{CSR}*	$\overline{\text{DISTR}}$/DISTR Delay from Chip Select	110	—	ns	
t_{WA}*	Address Hold Time from $\overline{\text{DOSTR}}$/DOSTR	50	—	ns	
t_{WCS}*	Chip Select Hold Time from $\overline{\text{DOSTR}}$/DOSTR	50	—	ns	
t_{AW}*	$\overline{\text{DOSTR}}$/DOSTR Delay from Address	160	—	ns	
t_{CSW}*	$\overline{\text{DOSTR}}$/DOSTR Delay from Select	160	—	ns	
t_{MRW}	Master Reset Pulse Width	25	—	μs	

*Applicable only when ADS input is tied permanently low.

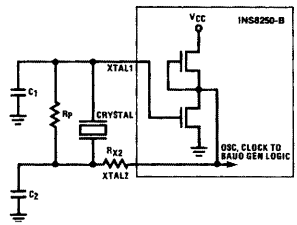
AC Electrical Characteristics (cont'd.)

Symbol	Parameter	Min	Max	Units	Test Conditions
BAUD GENERATOR					
N	Baud Rate Divisor	1	$2^{16}-1$		
t_{BLD}	Baud Output Negative Edge Delay		250 typ	ns	100 pF Load
t_{BHD}	Baud Output Positive Edge Delay		250 typ	ns	100 pF Load
t_{LW}	Baud Output Down Time	425 typ		ns	100 pF Load
t_{HW}	Baud Output Up Time	330 typ		ns	100 pF Load
RECEIVER					
t_{SCD}	Delay from RCLK to Sample Time		2 typ	μs	
t_{SINT}	Delay from Stop to Set Interrupt		2 typ	μs	100 pF Load
t_{RINT}	Delay from $\overline{DISTR}$/DISTR (RD RBR/RDLSR) to Reset Interrupt		1 typ	μs	100 pF Load
TRANSMITTER					
t_{HR}	Delay from $\overline{DOSTR}$/DOSTR (WR THR) to Reset Interrupt		1 typ	μs	100 pF Load
t_{IRS}	Delay from Initial INTR Reset to Transmit Start		16 typ	$\overline{BAUDOUT}$ Cycles	
t_{SI}	Delay from Initial Write to Interrupt		24 typ	$\overline{BAUDOUT}$ Cycles	
t_{SS}	Delay from Stop to Next Start		1 typ	μs	
t_{STI}	Delay from Stop to Interrupt (THRE)		8 typ	$\overline{BAUDOUT}$ Cycles	
t_{IR}	Delay from $\overline{DISTR}$/DISTR (RD IIR) to Reset Interrupt (THRE)		1 typ	μs	100 pF Load
MODEM CONTROL					
t_{MDO}	Delay from DOSTR/$\overline{DOSTR}$ (WR MCR) to Output		1 typ	μs	100 pF Load
t_{SIM}	Delay to Set Interrupt from MODEM Input		1 typ	μs	100 pF Load
t_{RIM}	Delay to Reset Interrupt from $\overline{DISTR}$/DISTR (RD MSR)		1 typ	μs	100 pF Load



Timing	Min	Units
t_{XH}	140	ns
t_{XL}	140	ns

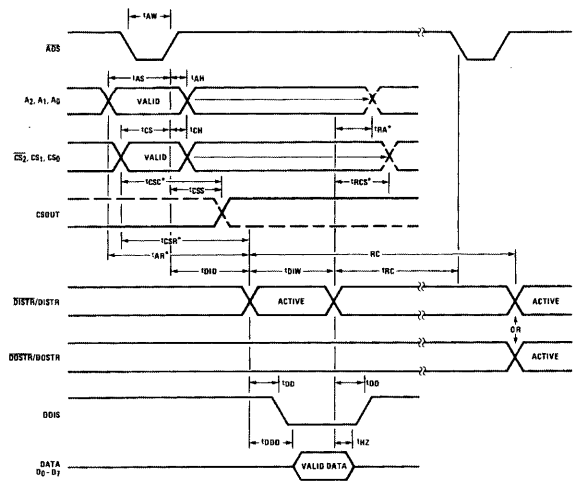
A. External Clock Input (3.1 MHz Max.)



CRYSTAL	R_P	R_{X2}	C_1	C_2
3.1 MHz	1 MΩ	1.5K	10 - 30 pF	40 - 60 pF

B. Typical Crystal Oscillator Network

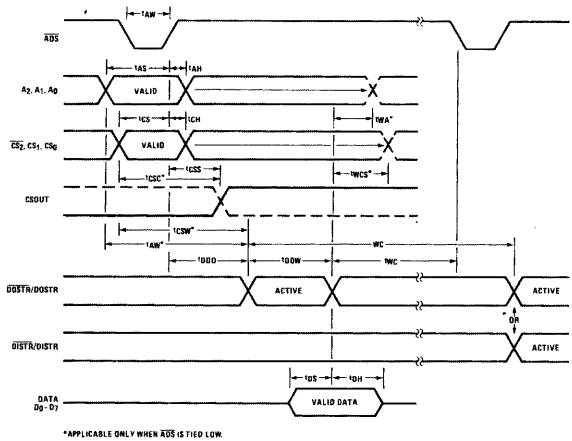
Timing Waveforms



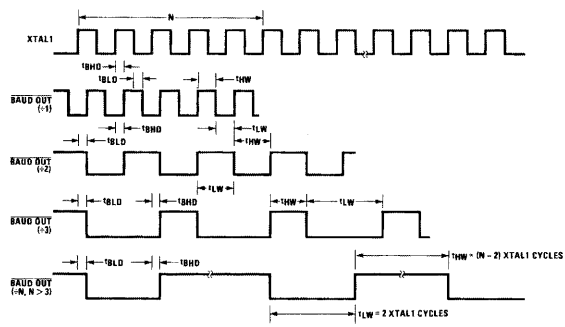
*APPLICABLE ONLY WHEN ADS IS TIED LOW.

Read Cycle

Timing Waveforms (cont'd.)

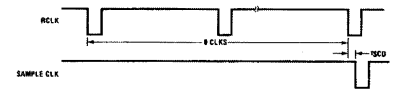


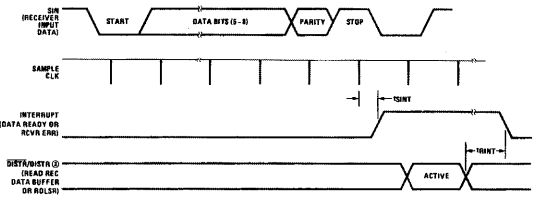
Write Cycle



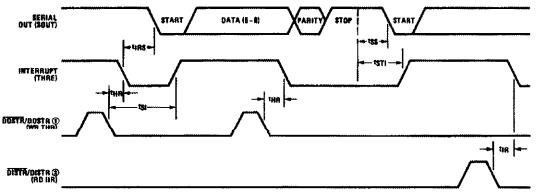
BAUDOUT Timing

Timing Waveforms (cont'd.)

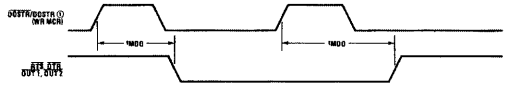


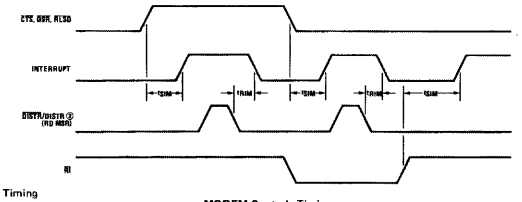


Receiver Timing



Transmitter Timing

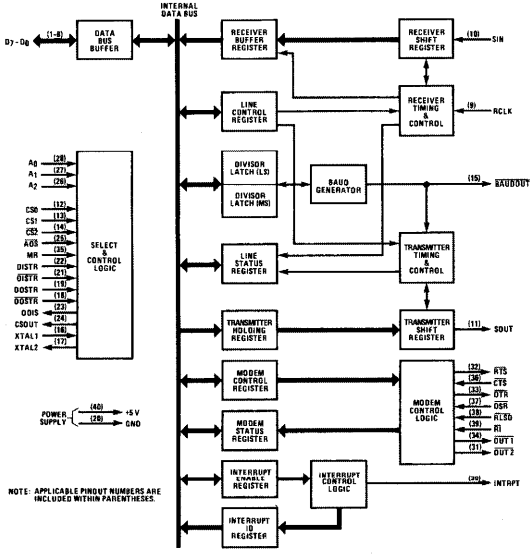




MODEM Controls Timing

NOTES:
① See Write Cycle Timing
② See Read Cycle Timing

INS8250-B Block Diagram



INS8250-B Functional Pin Description

The following describes the function of all INS8250 input/output pins. Some of these descriptions reference internal circuits.

NOTE

In the following descriptions, a low represents a logic 0 (0 volt nominal) and a high represents a logic 1 (+2.4 volts nominal).

INPUT SIGNALS

Chip Select (CS0, CS1, $\overline{CS2}$), Pins 12 – 14: When CS0 and CS1 are high and $\overline{CS2}$ is low, the chip is selected. Chip selection is complete when the decoded chip select signal is latched with an active (low) Address Strobe ($\overline{ADS}$) input. This enables communication between the INS8250 and the CPU.

Data Input Strobe (DISTR, $\overline{DISTR}$), Pins 22 and 21: When DISTR is high or $\overline{DISTR}$ is low while the chip is selected, allows the CPU to read status information or data from a selected register of the INS8250.

NOTE

Only an active DISTR or $\overline{DISTR}$ input is required to transfer data from the INS8250 during a read operation. Therefore, tie either the DISTR input permanently low or the $\overline{DISTR}$ input permanently high, if not used.

Data Output Strobe (DOSTR, $\overline{DOSTR}$), Pins 19 and 18: When DOSTR is high or $\overline{DOSTR}$ is low while the chip is selected, allows the CPU to write data or control words into a selected register of the INS8250.

NOTE

Only an active DOSTR or $\overline{DOSTR}$ input is required to transfer data to the INS8250 during a write operation. Therefore, tie either the DOSTR input permanently low or the $\overline{DOSTR}$ input permanently high, if not used.

Address Strobe ($\overline{ADS}$), Pin 25: When low, provides latching for the Register Select (A0, A1, A2) and Chip Select (CS0, CS1, $\overline{CS2}$) signals.

NOTE

An active $\overline{ADS}$ input is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, tie the $\overline{ADS}$ input permanently low.

Register Select (A0, A1, A2), Pins 26 – 28: These three inputs are used during a read or write operation to select an INS8250 register to read from or write into as indicated in the table below. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain INS8250 registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.

DLAB	A_2	A_1	A_0	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	None
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

Master Reset (MR), Pin 35: When high, clears all the registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches), and the control logic of the INS8250. Also, the state of various output signals (SOUT, INTRPT, $\overline{OUT1}$, $\overline{OUT2}$, $\overline{RTS}$, $\overline{DTR}$) are affected by an active MR input. (Refer to table 1.)

Receiver Clock (RCLK), Pin 9: This input is the 16x baud rate clock for the receiver section of the chip.

Serial Input (SIN), Pin 10: Serial data input from the communications link (peripheral device, MODEM, or data set).

Clear to Send ($\overline{CTS}$), Pin 36: The $\overline{CTS}$ signal is a MODEM control function input whose condition can be tested by the CPU by reading bit 4 (CTS) of the MODEM Status Register. Bit 0 (ΔCTS) of the MODEM Status Register indicates whether the $\overline{CTS}$ input has changed state since the previous reading of the MODEM Status Register.

NOTE

Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Data Set Ready ($\overline{DSR}$), Pin 37: When low, indicates that the MODEM or data set is ready to establish the communications link and transfer data with the INS8250. The $\overline{DSR}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 5 (DSR) of the MODEM Status Register. Bit 1 (DDSR) of the MODEM Status Register indicates whether the $\overline{DSR}$ input has changed state since the previous reading of the MODEM Status Register.

NOTE

Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Received Line Signal Detect ($\overline{RLSD}$), Pin 38: When low, indicates that the data carrier has been detected by the MODEM or data set. The $\overline{RLSD}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 7 (RLSD) of the MODEM Status Register. Bit 3 (DRLSD) of the MODEM Status Register indicates whether the $\overline{RLSD}$ input has changed state since the previous reading of the MODEM Status Register.

NOTE

Whenever the RLSD bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Ring Indicator ($\overline{RI}$), Pin 39: When low, indicates that a telephone ringing signal has been received by the MODEM or data set. The $\overline{RI}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 6 (RI) of the MODEM Status Register. Bit 2 (TERI) of the MODEM Status Register indicates whether the $\overline{RI}$ input has changed from a low to a high state since the previous reading of the MODEM Status Register.

NOTE

Whenever the RI bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status Interrupt is enabled.

V_{CC}, Pin 40: +5-volt supply.

V_{SS}, Pin 20: Ground (0-volt) reference.

OUTPUT SIGNALS

Data Terminal Ready ($\overline{DTR}$), Pin 33: When low, informs the MODEM or data set that the INS8250 is ready to communicate. The DTR output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. The $\overline{DTR}$ signal is set high upon a Master Reset operation.

Request to Send ($\overline{RTS}$), Pin 32: When low, informs the MODEM or data set that the INS8250 is ready to transmit data. The $\overline{RTS}$ output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. The $\overline{RTS}$ signal is set high upon a Master Reset operation.

Output 1 ($\overline{OUT1}$), Pin 34: User-designated output that can be set to an active low by programming bit 2 ($\overline{OUT1}$) of the MODEM Control Register to a high level. The $\overline{OUT1}$ signal is set high upon a Master Reset operation.

Output 2 ($\overline{OUT2}$), Pin 31: User-designated output that can be set to an active low by programming bit 3 ($\overline{OUT2}$) of the MODEM Control Register to a high level. The $\overline{OUT2}$ signal is set high upon a Master Reset operation.

Chip Select Out (CSOUT), Pin 24: When high, indicates that the chip has been selected by active CS0, CS1, and $\overline{CS2}$ inputs. No data transfer can be initiated until the CSOUT signal is a logic 1.

Driver Disable (DDIS), Pin 23: Goes low whenever the CPU is reading data from the INS8250. A high-level DDIS output can be used to disable an external transceiver (if used between the CPU and INS8250 on the D_7 - D_0 Data Bus) at all times, except when the CPU is reading data.

Baud Out ($\overline{BAUDOUT}$), Pin 15: 16x clock signal for the transmitter section of the INS8250. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. The $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to the RCLK input of the chip.

Interrupt (INTRPT), Pin 30: Goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag; Received Data Available; Transmitter Holding Register Empty; and MODEM Status. The INTRPT signal is reset low upon the appropriate interrupt service or a Master Reset operation.

Serial Output (SOUT), Pin 11: Composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state upon a Master Reset operation.

INPUT/OUTPUT SIGNALS

Data (D_7 - D_0) Bus, Pins 1 - 8: This bus comprises eight TRI-STATE input/output lines. The bus provides bidirectional communications between the INS8250 and the CPU. Data, control words, and status information are transferred via the D_7 - D_0 Data Bus.

External Clock Input/Output (XTAL 1, XTAL 2), Pins 16 and 17: These two pins connect the main timing reference (crystal or signal clock) to the INS8250.

Pin Configuration

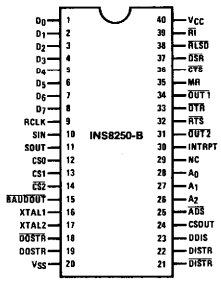


Table 1. ACE Reset Functions

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	All Bits Low (0 - 3 forced and 4 - 7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1 and 2 Low Bits 3 - 7 are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, Except Bits 5 & 6 are High
MODEM Status Register	Master Reset	Bits 0 - 3 Low Bits 4 - 7 — Input Signal
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read RBR/MR	Low
INTRPT (THRE)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read MSR/MR	Low
$\overline{OUT\ 2}$	Master Reset	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
$\overline{OUT\ 1}$	Master Reset	High

INS8250-B Accessible Registers

The system programmer may access or control any of the INS8250 registers summarized in table 2 via the CPU. These registers are used to control INS8250 operations and to transmit and receive data.

INS8250 LINE CONTROL REGISTER

The system programmer specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the programmer may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The contents of the Line Control Register are indicated in table 2 and are described below.

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits in each transmitted or received serial character. If bit 2 is a logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, 1½ Stop bits are generated or checked. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated or checked.

Table 2. Summary of INS8250-B Accessible Registers

	Register Address									
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	3	4	5	6	0 DLAB = 1	1 DLAB = 1
Bit No.	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Identification Register (Read Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Divisor Latch (LS)	Divisor Latch (MS)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	DLL	DLM
0	Data Bit 0*	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OR)	Delta Data Set Ready (DDSR)	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Receive Line Signal Detect (DRLSD)	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Shift Register Empty (TSRE)	Ring Indicator (RI)	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Received Line Signal Detect (RLSD)	Bit 7	Bit 15

* Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver as a logic 0 if bit 4 is a logic 1 or as a logic 1 if bit 4 is a logic 0.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state and remains there regardless of other transmitter activity. The set break is disabled by setting bit 6 to a logic 0. This feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

INS8250 PROGRAMMABLE BAUD RATE GENERATOR

The INS8250 contains a programmable Baud Rate Generator that is capable of taking any clock input (DC to 3.1 MHz) and dividing it by any divisor from 1 to $(2^{16}-1)$. The output frequency of the Baud Generator is 16x the Baud rate [divisor # = (frequency input) ÷ (baud rate x 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 3 and 4 illustrate the use of the Baud Rate Generator with crystal frequencies of 1.8432 MHz and 3.072 MHz respectively. For baud rates of 38400 and below the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen.

NOTE

The maximum operating frequency of the Baud Generator is 3.1 MHz. However, when using divisors of 3 and below, the maximum frequency is equal to the divisor in MHz. For example, if the divisor is 1, then the maximum frequency is 1 MHz. In no case should the data rate be greater than 56k Baud.

LINE STATUS REGISTER

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in table 2 and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 may be reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register or by writing a logic 0 into it from the CPU.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Table 3. Baud Rates Using 1.8432 MHz Crystal

Desired Baud Rate	Divisor Used to Generate 16x Clock	Percent Error Difference Between Desired & Actual
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.86

NOTE: 1.8432 MHz is the standard 8080 frequency divided by 10.

Table 4. Baud Rates Using 3.072 MHz Crystal

Desired Baud Rate	Divisor Used to Generate 16x Clock	Percent Error Difference Between Desired & Actual
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.23
9600	20	–
19200	10	–
38400	5	–

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level).

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits).

NOTE

Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the INS8250 is ready to accept a new character for transmission. In addition, this bit causes the INS8250 to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Shift Register Empty (TSRE) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Shift Register is idle. It is reset to logic 0 upon a data transfer from the Transmitter Holding Register to the Transmitter Shift Register. Bit 6 is a read-only bit.

Bit 7: This bit is permanently set to logic 0.

INTERRUPT IDENTIFICATION REGISTER

The INS8250 has an on-chip interrupt capability that allows for complete flexibility in interfacing to all the popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the INS8250 prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and the type of that interrupt are stored in the Interrupt Identification Register (refer to table 5). The Interrupt Identification Register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in table 2 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in table 5.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Table 5. Interrupt Control Functions

Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	1	–	None	None	–
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

INTERRUPT ENABLE REGISTER

This 8-bit register enables the four types of interrupts of the INS8250 to separately active the chip Interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are indicated in table 2 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

MODEM CONTROL REGISTER

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in table 2 and are described below.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

NOTE

The $\overline{DTR}$ output of the INS8250 may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 ($\overline{OUT\,1}$) signal, which is an auxiliary user-designated output. Bit 2 affects the $\overline{OUT\,1}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 ($\overline{OUT\,2}$) signal, which is an auxiliary user-designated output. Bit 3 affects the $\overline{OUT\,2}$ output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a loopback feature for diagnostic testing of the INS8250. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$, and $\overline{RI}$) are disconnected; and the four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\,1}$, and $\overline{OUT\,2}$) are internally connected to the four MODEM Control inputs. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the INS8250.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The INS8250 interrupt system can be tested by writing into the lower six bits of the Line Status Register and the lower four bits of the MODEM Status Register. Setting any of these bits to a logic 1 generates the appropriate interrupt (if enabled). The resetting of these interrupts is the same as in normal INS8250 operation. To return to normal operation, the registers must be reprogrammed for normal operation and then bit 4 of the MODEM Control Register must be reset to logic 0.

Bits 5 through 7: These bits are permanently set to logic 0.

MODEM STATUS REGISTER

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in table 2 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the $\overline{RLSD}$ input to the chip has changed state.

NOTE

Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR.

Bit 7: This bit is the complement of the Received Line Signal Detect ($\overline{RLSD}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 2 of the MCR.

Typical Applications

Figures 1 and 2 show how to use the INS8250 chip in an INS8080A system and in a microcomputer system with a high-capacity data bus.

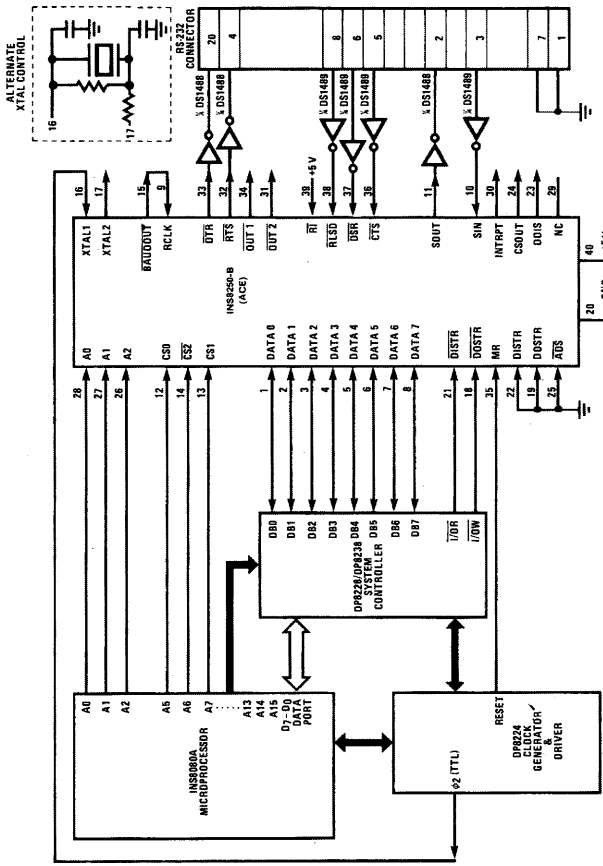


Figure 1. Typical INS8080A/INS8250-B RS-232 Terminal Interface

Typical Applications (cont'd)

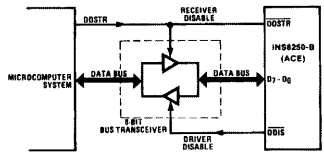
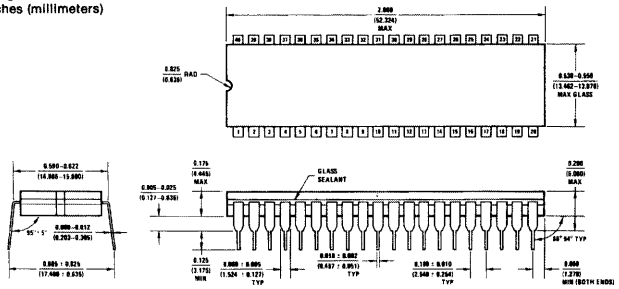


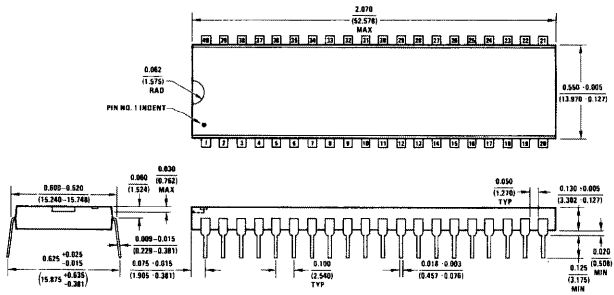
Figure 2. Typical Interface for a High-Capacity Data Bus

Physical Dimensions

inches (millimeters)



Ceramic Dual-In-Line Package [Cerdip (J)]
Order Number INS8250J-B



Plastic Dual-In-Line Package (N)
Order Number INS8250N-B

National Semiconductor Corporation
2900 Semiconductor Drive
Santa Clara, CA. 95051
Tel: (408)737-5000
TWX: (910)339-9240

National Semiconductor GmbH
Eisenheimerstrasse 61/111
8000 Munchen 21
West Germany
Tel: (089)576091
Telex: 05-22772

NS International Inc., Japan
Miyake Building
1-9 Yotsuya Shinjuku-ku 160
Tokyo, Japan
Tel: (03)355-3711
TWX: 232-2015 NSCJ—J

National Semiconductor (Hong Kong) Ltd.
8th Floor
Cheung Kong Electronic Bldg.
4 Hing Yip Street
Kwun Tong
Kowloon, Hong Kong
Tel: 3-899235
Telex: 73866 NSEHK HX
Cable: NATSEMI

NS Electronics Do Brasil
Avda Brigadeiro Faria Lima 844
11 Andar Conjunto 1104
Jardim Paulistano
Sao Paulo, Brasil
Telex 1121008 Cable Sao Paulo

NS Electronics Pty. Ltd.
Cnr. Stud Rd. & Mtn. Highway
Bayswater, Victoria 3153
Australia
Tel: 03-729-6333
Telex: 32096

OKI semiconductor

MSM6242RS/GS

DIRECT BUS CONNECTED CMOS REAL TIME CLOCK/CALENDAR

GENERAL DESCRIPTION

The MSM6242 is a silicon gate CMOS Real Time Clock/Calendar for use in direct bus-connection Microprocessor/Microcomputer applications. An on-chip 32.768KHz crystal oscillator time base is divided to provide addressable 4-bit I/O data for SECONDS, MINUTES, HOURS, DAY OF WEEK, DATE, MONTH and YEAR. Data access is controlled by 4-bit address, chip selects ($\overline{CS0}$, CS1), $\overline{WRITE}$, $\overline{READ}$, and ALE. Control Registers D, E and F provide for 30 SECOND error adjustment, INTERRUPT REQUEST (IRQ FLAG) and BUSY status bits, clock STOP, HOLD, and RESET FLAG bits, 4 selectable INTERRUPTS rates are available at the STD.P (STANDARD PULSE) output utilizing Control Register inputs T0, T1 and the ITRPT/STND (INTERRUPT/STANDARD). Masking of the interrupt output (STD.P) can be accomplished via the MASK bit. The MSM6242 can operate in a 12/24 hour format and Leap Year timing is automatic.

The MSM6242 normally operates from a 5V ± 10% supply at −30 to 85°C. Battery backup operation down to 2.0V allows continuation of time keeping when main power is off. The MSM6242 is offered in a 18-pin plastic DIP and FLAT package.

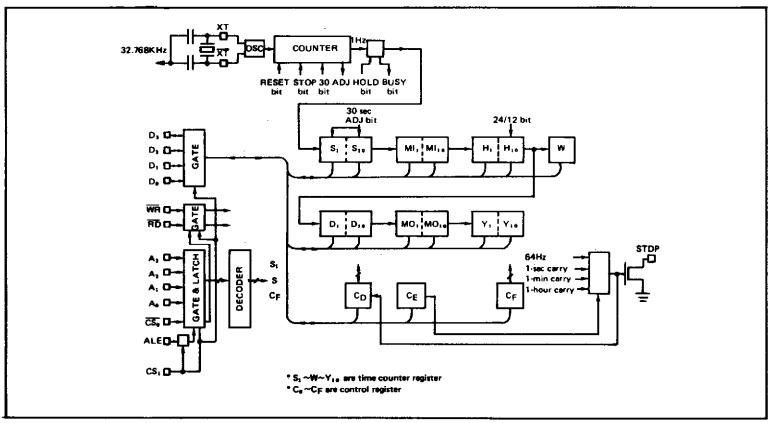
FEATURES

DIRECT MICROPROCESSOR/MICROCONTROLLER BUS CONNECTION

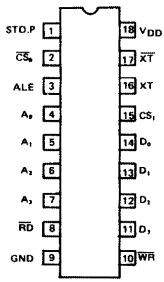
TIME	MONTH	DATE	YEAR	DAY OF WEEK
23:59:59	12	31	80	7

- 4-bit data bus
- 4-bit address bus
- $\overline{READ}$, $\overline{WRITE}$, ALE and CHIP SELECT INPUTS
- Status registers — IRQ and BUSY
- Selectable interrupt outputs — 1/64 second, 1 second, 1 minute, 1 hour
- Interrupt masking
- 32.768KHz crystal controlled operation
- 12/24 hour format
- Auto leap year
- ±30 second error correction
- Single 5V supply
- Battery backup down to V_{DD} = 2.0V
- Low power dissipation:
  20 μW max at V_{DD} = 2V
  150 μW max at V_{DD} = 5V
- 18-pin plastic DIP package

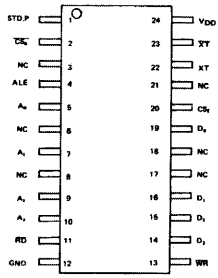
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



18 pin Plastic DIP Package



24 pin Plastic Flat Package

A0-A3:	Address input
D0-D3:	Data input/output
$\overline{CS0}$, $\overline{CS1}$	CHIP SELECTS 0, 1
$\overline{RD}$:	READ enable
$\overline{WR}$:	WRITE enable
ALE:	Address latch enable
STD.P:	Standard pulse output
XT, $\overline{XT}$:	XTAL oscillator input/output
VDD:	+5V supply
VSS:	ground

REGISTER TABLE

Address Input	Address Input				Register Name	Data				Count value	Description
	A_3	A_2	A_1	A_0		D_3	D_2	D_1	D_0		
0	0	0	0	0	S_1	S_8	S_4	S_2	S_1	0 ~ 9	1-second digit register
1	0	0	0	1	S_{10}	*	S_{40}	S_{20}	S_{10}	0 ~ 5	10-second digit register
2	0	0	1	0	MI_1	mi_8	mi_4	mi_2	mi_1	0 ~ 9	1-minute digit register
3	0	0	1	1	MI_{10}	*	mi_{40}	mi_{20}	mi_{10}	0 ~ 5	10-minute digit register
4	0	1	0	0	H_1	h_8	h_4	h_2	h_1	0 ~ 9	1-hour digit register
5	0	1	0	1	H_{10}	*	PM/AM	h_{20}	h_{10}	0 ~ 2 or 0 ~ 1	PM/AM, 10-hour digit register
6	0	1	1	0	D_1	d_8	d_4	d_2	d_1	0 ~ 9	1-day digit register
7	0	1	1	1	D_{10}	*	*	d_{20}	d_{10}	0 ~ 3	10-day digit register
8	1	0	0	0	MO_1	mo_8	mo_4	mo_2	mo_1	0 ~ 9	1-month digit register
9	1	0	0	1	MO_{10}	*	*	*	MO_{10}	0 ~ 1	10-month digit register
A	1	0	1	0	Y_1	y_8	y_4	y_2	y_1	0 ~ 9	1-year digit register
B	1	0	1	1	Y_{10}	y_{80}	y_{40}	y_{20}	y_{10}	0 ~ 9	10-year digit register
C	1	1	0	0	W	*	w_4	w_2	w_1	0 ~ 6	Week register
D	1	1	0	1	C_D	30 sec. ADJ	IRQ FLAG	BUSY	HOLD	–	Control Register D
E	1	1	1	0	C_E	t_1	t_0	ITRPT /STND	MASK	–	Control Register E
F	1	1	1	1	C_F	TEST	24/12	STOP	REST	–	Control Register F

REST = RESET
ITRPT/STND = INTERRUPT/STANDARD

Note 1) – Bit * does not exist (unrecognized during a write and held at "0" during a read).
Note 2) – Be sure to mask the AM/PM bit when processing 10's of hour's data.
Note 3) – BUSY bit is read only. The IRQ FLAG bit can only be set to a "0". Setting the IRQ FLAG to a "1" is done by hardware.

Figure 1. Register Table

OSCILLATOR FREQUENCY DEVIATIONS

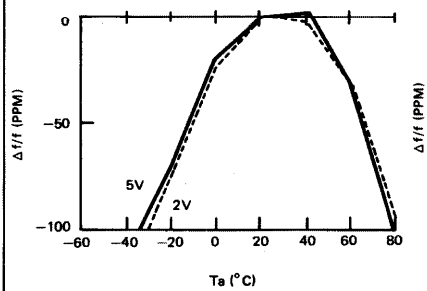


Figure 2. Frequency Deviation (PPM) vs Temperature

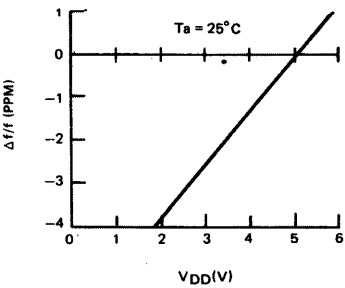
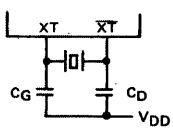


Figure 3. Frequency Deviation (PPM) vs Voltage

Note: 1. The graphs above showing frequency deviation vs temperature/voltage are primarily characteristic of the MSM6242 with the oscillation circuit described below.



Crystal: Type N_6, P_3 by kinseki (32.768 KHz)

C_G, C_D: 22pF (Temperature Characteristics: 0)

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	−0.3~ 7	V
Input Voltage	V_I		GND − 0.3~V_{DD} + 0.3	V
Output Voltage	V_O		GND − 0.3~V_{DD} + 0.3	V
Storage Temperature	T_{STG}		−55~ +150	°C

OPERATING CONDITIONS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	–	4 ~ 6	V
Standby Supply Voltage	V_{BAK}	–	2 ~ 6	
Crystal Frequency	$f_{(XT)}$	–	32.768	kHz
Operating Temperature	T_{OP}	–	−30~+85	°C

D.C. CHARACTERISTICS

V_{DD} = 5V ± 10%, T_A = −30 ~ +85

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable Terminal
"H" Input Voltage	$V_{IH}1$	–	2.2	–	–	V	All input terminals except CS_1
"L" Input Voltage	$V_{IL}1$	–	–	–	0.8		
Input Leak Current	$I_{LK}1$	V_I = V_{DD}/0V	–	–	1/−1	μA	Input terminals other than D_0 ~ D_3
Input Leak Current	$I_{LK}2$		–	–	10/−10		D_0 ~ D_3
"L" Output Voltage	$V_{OL}1$	I_{OL} = 2.5mA	–	–	0.4	V	D_0 ~ D_3
"H" Output Voltage	V_{OH}	I_{OH} = −400μA	2.4	–	–		
"L" Output Voltage	$V_{OL}2$	I_{OL} = 2.5mA	–	–	0.4	V	STD.P
OFF Leak Current	I_{OFFLK}	V = V_{DD}/0V	–	–	10	μA	
Input Capacitance	C_I	Input frequency 1MHz	–	5	–	PF	All input terminals
Current Consumption	$I_{DD}1$	$f_{(xt)}$ = 32.768 KHz, T_a=25°C, V_{DD} = 5V	–	–	30	μA	V_{DD}
Current Consumption	$I_{DD}2$	$f_{(xt)}$ = 32.768 KHz, T_a=25°C, V_{DD} = 2V	–	–	10		
"H" Input Voltage	$V_{IH}2$	V_{DD} = 2~5.5V	4/5V_{DD}	–	–	V	CS_1
"L" Input Voltage	$V_{IL}2$		–	–	1/5V_{DD}		

SWITCHING CHARACTERISTICS

(1) WRITE mode (ALE = V_{DD})

(V_{DD} = 5V ± 10% = Ta = −30 ~ +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
CS_1 Set up Time	t_{C1S}	–	1000	–	ns
CS_1 Hold Time	t_{C1H}	–	1000	–	
Address Stable Before WRITE	t_{AW}	–	100	–	
Address Stable After WRITE	t_{WA}	–	10	–	
WRITE Pulse Width	t_{WW}	–	250	–	
Data Set up Time	t_{DS}	–	180	–	
Data Hold Time	t_{DH}	–	10	–	

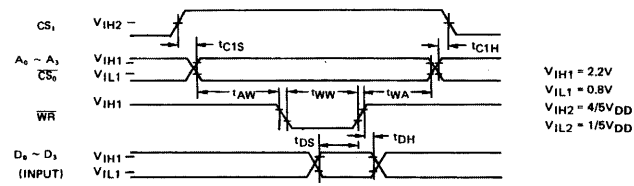


Figure 4. Write Cycle – (ALE = VDD)

(2) WRITE mode (With use of ALE)

(V_{DD} = 5 V ± 10%, Ta = −3C)

Parameter	Symbol	Condition	Min.	Max.	Unit
CS_1 Set up Time	t_{CIS}	–	1000	–	ns
Address Set up Time	t_{AS}	–	50	–	
Address Hold Time	t_{AH}	–	50	–	
ALE Pulse Width	t_{AW}	–	80	–	
ALE Before WRITE	t_{ALW}	–	0	–	
WRITE Pulse Width	t_{WW}	–	250	–	
ALE After WRITE	t_{WAL}	–	50	–	
DATA Set up Time	t_{DS}	–	180	–	
DATA Hold Time	t_{DH}	–	10	–	
CS_1 Hold Time	t_{C1H}	–	1000	–	

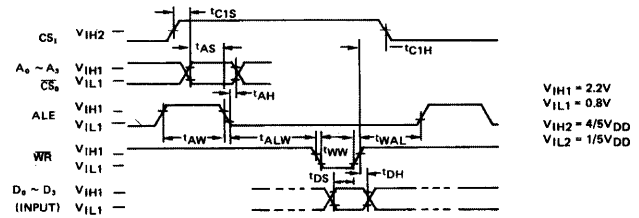


Figure 5. Write Cycle – (With Use of ALE)

(3) READ mode (ALE = V_{DD})

(V_{DD} = 5V ± 10%, Ta = –30 ~ +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
$\overline{CS_1}$ Set up Time	t_{C1S}	–	1000	–	ns
CS_1 Hold Time	t_{C1H}	–	1000	–	
Address Stable Before READ	t_{AR}	–	80	–	
Address Stable After READ	t_{RA}	–	0	–	
$\overline{RD}$ to Data	t_{RD}	C_L = 150pF	–	280	
Data Hold	t_{DR}	–	0	–	

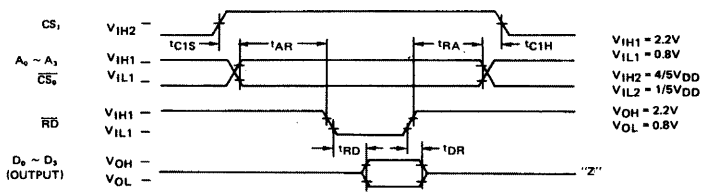


Figure 6. Read Cycle – (ALE = VDD)

(4) READ mode (With use of ALE)

(V_{DD} = 5V ±10%, Ta = −30~+85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
CS_1 Set up Time	t_{C1S}	–	1000	–	ns
Address Set up Time	t_{AS}	–	50	–	
Address Hold Time	t_{AH}	–	50	–	
ALE Pulse Width	t_{AW}	–	80	–	
ALE Before READ	t_{ALR}	–	0	–	
ALE after READ	t_{RAL}	–	0	–	
RD to Data	t_{RD}	C_L = 150pF	–	280	
DATA Hold	t_{DR}	–	0	–	
CS_1 Hold Time	t_{C1H}	–	1000	–	

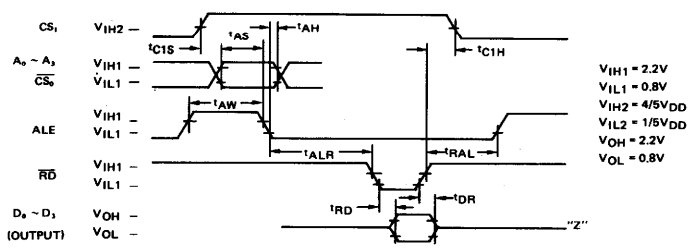
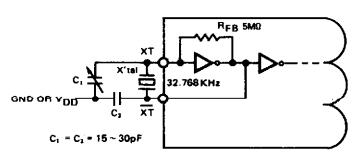


Figure 7. Read Cycle – (With Use of ALE)

PIN DESCRIPTION

Name	Pin No. RS	Pin No. GS	Description
D_0	14	19	Data Input/Output pins to be directly connected to a microcontroller bus for reading and writing of the clock/calendar's registers and control registers. D0 = LSB and D3 = MSB.
D_1	13	16	
D_2	12	15	
D_3	11	14	
A_0	4	5	Address input pin for use by a microcomputer to select internal clock/calendar's registers and control registers for Read/Write operations (See Function Table Figure 1). Address input pins A0-A3 are used in combination with ALE for addressing registers.
A_1	5	7	
A_2	6	9	
A_3	7	10	
ALE	3	4	Address Latch Enable pin. This pin enables writing of address data when ALE = 1 and $\overline{CS0}$ = 0; address data is latched when ALE = 0 Microcontroller/Microprocessors having an ALE output should connect to this pin; otherwise it should be connected at V_{DD}.
$\overline{WR}$	10	13	Writing of data is performed by this pin. When CS_1 = 1 and $\overline{CS_0}$ = 0, $D_0 \sim D_3$ data is written into the register at the rising edge of $\overline{WR}$.
$\overline{RD}$	8	11	Reading of register data is accomplished using this pin. When CS_1 = 1, $\overline{CS_0}$ = 0 and $\overline{RD}$ = 0, the data of the register is output to $D_0 \sim D_3$. If both $\overline{RD}$ and $\overline{WR}$ are set at 0 simaltanuously, $\overline{RD}$ is to be inhibited.
$\overline{CS_0}$	2	2	Chip Select Pins. These pins enable/disable ALE, $\overline{RD}$ and $\overline{WR}$ operation. $\overline{CS_0}$ and ALE work in combination with one another, while CS_1 work independent with ALE. CS_1 must be connected to power failure detection as shown in Figure 18.
CS_1	15	20	
STD.P	1	1	Output pin of N-CH OPEN DRAIN type. The output data is controlled by the D_1 data content of C_E register. This pin has a priority to $\overline{CS_0}$ and CS_1. Refer to Figure 9 and FUNCTIONAL DESCRIPTION OF REGISTERS.
XT	16	22	32.768 kHz crystal is to be connected to these pins. When an external clock of 32.768 kHz is to be used for MSM6242's oscillation source, either CMOS output or pull-up TTL output is to be input from XT, while $\overline{XT}$ should be left open.
$\overline{XT}$	17	23	
V_{DD}	18	24	Power supply pin. +2 ~ +6V power is to be applied to this pin.
GND	9	12	Ground pin.



The impedance of the crystal should be less than 30kΩ

Figure 8. Oscillator Circuit

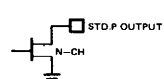


Figure 9.

FUNCTIONAL DESCRIPTION OF REGISTERS

■ $S_1, S_{10}, MI_1, MI_{10}, H_1, H_{10}, D_1, D_{10}, M\overline{O}_1, M\overline{O}_{10}, Y_1, Y_{10}, W$

a) These are abbreviations for SECOND1, SECOND10, MINUTE1, MINUTE10, HOUR1, HOUR10, DAY1, DAY10, MONTH1, MONTH10, YEAR1, YEAR10, and WEEK. These values are in BCD notation.

b) All registers are logically positive. For example, (S8, S4, S2, S1) = 1001 which means 9 seconds.

c) If data is written which is out of the clock register data limits, it can result in erroneous clock data being read back.

d) PM/AM, h_{20}, h_{10}
In the mode setting of 24-hour mode, PM/AM bit is ignored, while in the setting of 12-hour mode h_{20} is to be set. Otherwise it causes a discrepancy. In reading out the PM/AM bit in the 24-hour mode, it is continuously read out as 0. In reading out h_{20} bit in the 12-hour mode, 0 is written into this bit first, then it is continuously read out as 0 unless 1 is being written into this bit.

e) Registers Y1, Y10, and Leap Year. The MSM6242 is designed exclusively for the Christian Era and is capable of identifying a leap year automatically. The result of the setting of a non-existant day of the month is shown in the following example: If the date February 29 or November 31, 1985, was written, it would be changed automatically to March 1, or December 1, 1985 at the exact time at which a carry pulse occurs for the day's digit.

f) The Register W data limits are 0–6 (Table 1 shows a possible data definition).

TABLE 1

W_4	W_2	W_1	Day of Week
0	0	0	Sunday
0	0	1	Monday
0	1	0	Tuesday
0	1	1	Wednesday
1	0	0	Thursday
1	0	1	Friday
1	1	0	Saturday

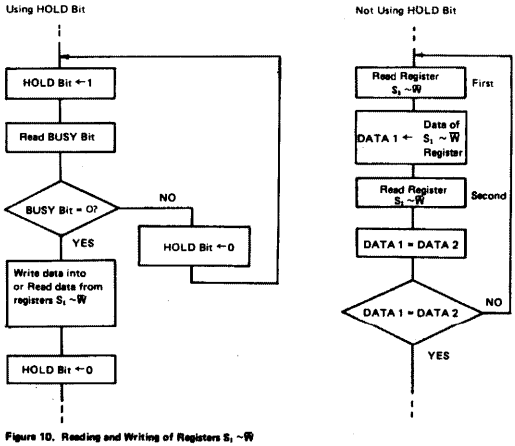
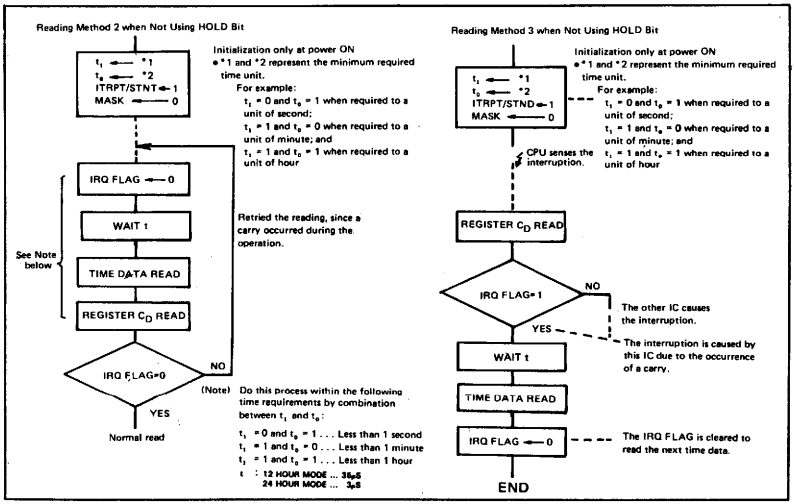


Figure 10. Reading and Writing of Registers $S_1 \sim \overline{W}$



■ CD REGISTER (Control D Register)

a) HOLD (D0) – Setting this bit to a "1" inhibits the 1Hz clock to the S1 counter, at which time the Busy status bit can be read. When Busy = 0, register's $S_1 \sim \overline{W}$ can be read or written. During this procedure if a carry occurs the S1 counter will be incremented by 1 second after HOLD = 0 (this condition is guaranteed as long as HOLD = 1 does not exceed 1 second in duration). If CS1 = 0 then HOLD = 0 irrespective of any condition.

b) BUSY (D1) – Status bit which shows the interface condition with microcontroller/microprocessors. As for the method of writing into and reading from $S_1 \sim \overline{W}$ (address $\phi \sim C$), refer to the flow chart described in Figure 10.

c) IRQ FLAG (D2) – This status bit corresponds to the output level of the STD.P output. When STD.P = 0, then IRQ = 1; when STD.P=1, then IRQ = 0. The IRQ FLAG indicates that an interrupt has occurred to the microcomputer if IRQ = 1. When D0 of register C_E (MASK) = 0, then the STD.P output changes according to the timing set by D3 (t_1) and D2 (t_0) of register E. When D1 of register E (ITRPT/STND) = 1 (interrupt mode), the STD.P output remains low until the IRQ FLAG is written to a "0". When IRQ = 1 and timing for a new interrupt occurs, the new interrupt is ignored. When ITRPT/STND = 0 (Standard Pulse Output mode) the STD.P output remains low until either "0" is written to the IRQ FLAG; otherwise, the IRQ FLAG automatically goes to "0" after 7.8125 ms.

When writing the HOLD or 30 second adjust bits of register D, it is necessary to write the IRQ FLAG bit to a "1".

d) ±30 ADJ (D3) – When 30-second adjustment is necessary, a "1" is written to bit D3 during which time the internal clock registers should not be read from or written to 125μs after bit D3 = 1 it will automatically return to a "0", and at that time reading or writing of registers can occur.

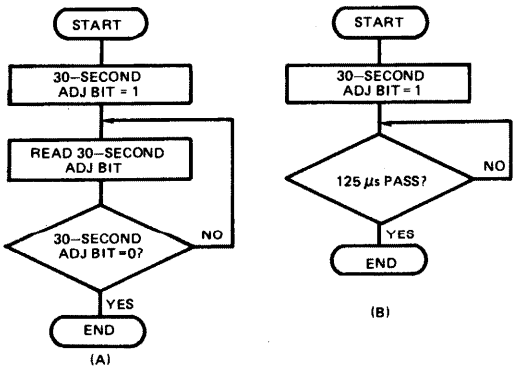


Figure 11. Writing 30-Second Adj. bit (Two Ways A, B)

■ CE REGISTER (Control E Register)

a) MASK (D0) – This bit controls the STD.P output. When MASK = 1, then STD.P = 1 (open); when MASK = 0, then STD.P = output mode. The relationship between the MASK bit and STD.P output is shown Figure 12.

b) INTRPT/STND (D1) – The INTRPT/STND input is used to switch the STD.P output between its two modes of operation, interrupt and Standard timing waveforms. When INTRPT/STND 0 a fixed cycle waveform with a low-level pulse width of 7.8125 ms is present at the STD.P output. At this time the MASK bit must equal 0, while the period in either mode is determined by T0(D2) and T1(D3) of Register E.

c) T0 (D2), T1 (D3) – These two bits determine the period of the STD.P output in both Interrupt and Fixed timing waveform modes. The tables below show the timing associated with the T0, T1 inputs as well as their relationship to INTRPT/STND and STD.P.

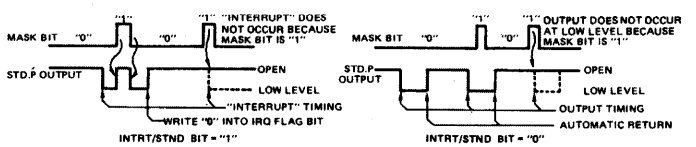
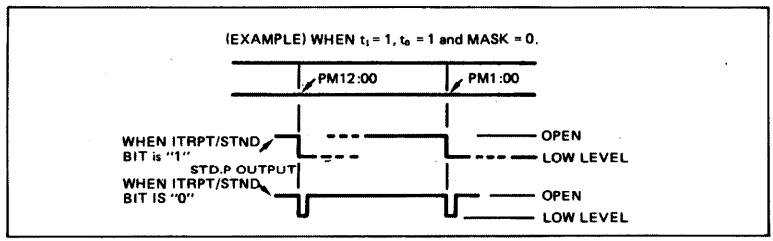


Figure 12.

t_1	t_0	Period	Duty CYCLE of "0" level when ITRPT/STND bit is "0".
0	0	1/64 second	1/2
0	1	1 second	1/128
1	0	1 minute	1/7680
1	1	1 hour	1/460800

TABLE 2

The timing of the STD.P output designated by T1 and T0 occurs the moment that a carry occurs to a clock digit.



d) The low-level pulse width of the fixed cycle waveform (ITRPT/STND = 0) is 7.8125 ms independent of T0/T1 inputs.

e) The fixed cycle waveform mode can be used for adjustment of the oscillator frequency time base. (See Figure 14).

f) During ±30 second adjustment a carry can occur that will cause the STD.P output to go low when T0/T1 = 1,0 or 1,1. However, when T1/T0 = 0, 0 and ITRPT/STND = 0, carry does not occur and the STD.P output resumes normal operation.

g) The STD.P output is held (frozen) at the point at which STOP = 1 while ITRPT/STND = 0.

h) No STD.P output change occurs as a result of writing data to registers S1 ~ H1.

■ C_F REGISTER (Control F Register)

a) REST (D0) – "RESET" — This bit is used to clear the clock's internal divider/counter of less than a second. When REST = 1, the counter is Reset for the duration of REST. In order to release this counter from Reset, a "0" must be written to the REST bit. If $\overline{CSO}$ = 0 then REST = 0 automatically.

b) STOP (D1) – The STOP FLAG Only inhibits carries into the 8192Hz divider stage. There may be up to 122μs delay before timing starts or stops after changing this flag; 1 = STOP/0 = RUN.

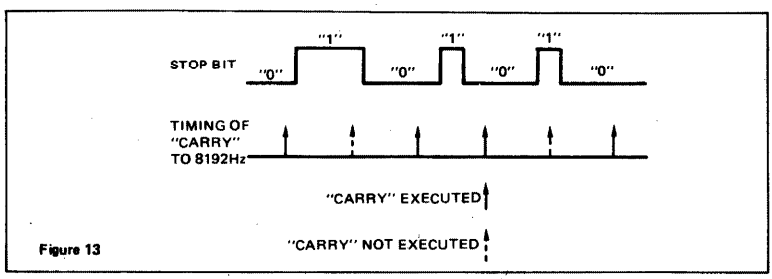


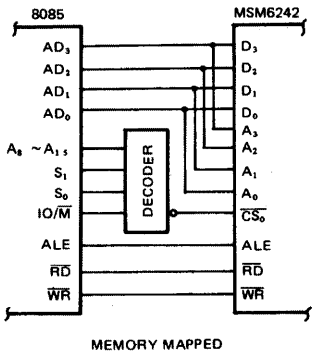
Figure 13

c) 24/12 (D2) – This bit is for selection of 24/12 hour time modes. If D2 = 1—24 hour mode is selected and the PM/AM bit is invalid. If D2 = 0—12 hour mode is selected and the PM/AM bit is valid.

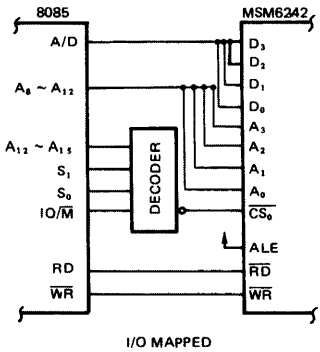
"24 HOUR/ 12 HOUR" — Setting of the 24/12 hour bit is as follows:
1) REST bit = 1
2) 24/12 hour bit = 0 or 1
3) REST bit = 0
* REST bit must = 1 to write to the 24/12 hour bit.

d) TEST (d3) – When the TEST flag is a "1", the input to the SECONDS counter comes from the counter/divider stage instead of the 15th divider stage. This makes the SECONDS counter count at 5.4163KHz instead of 1Hz. When TEST = 1 (Test Mode) the STOP & REST (Reset) flags do not inhibit internal counting. When Hold = 1 during Test (Test = 1) internal counting is inhibited; however, when the HOLD FLAG goes inactive (Hold = 0) counter updating is not guaranteed.

TYPICAL APPLICATION INTERFACE WITH MSM6242 AND MICROCONTROLLERS



MEMORY MAPPED



I/O MAPPED

Figure 15.

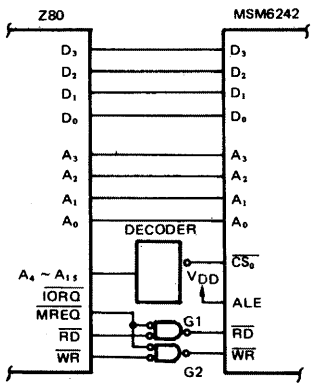


Figure 16.

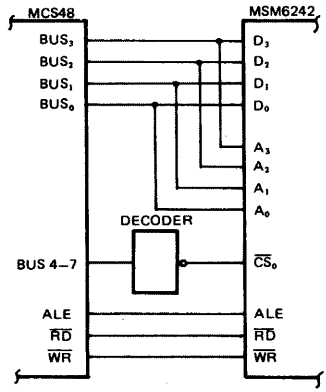


Figure 17.

TYPICAL APPLICATIONS – INTERFACE WITH MSM80C49

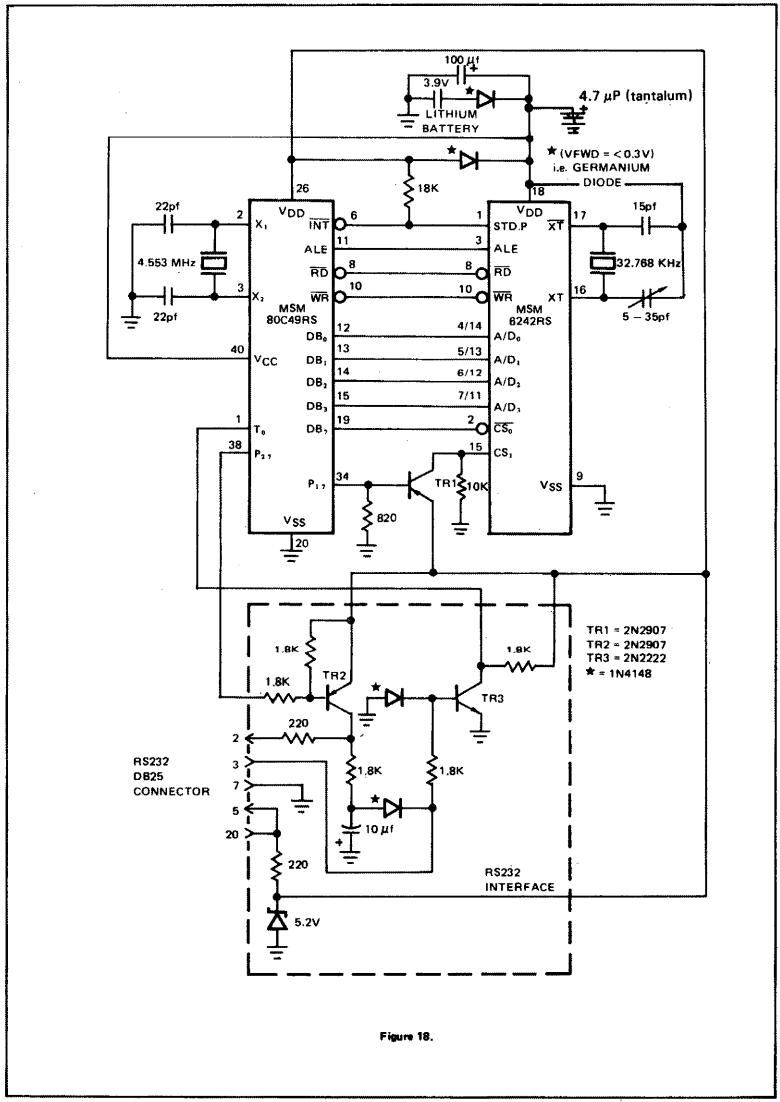
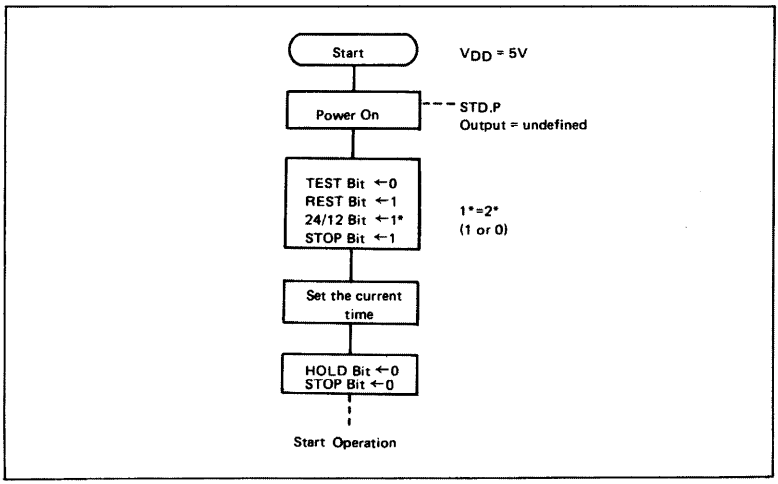


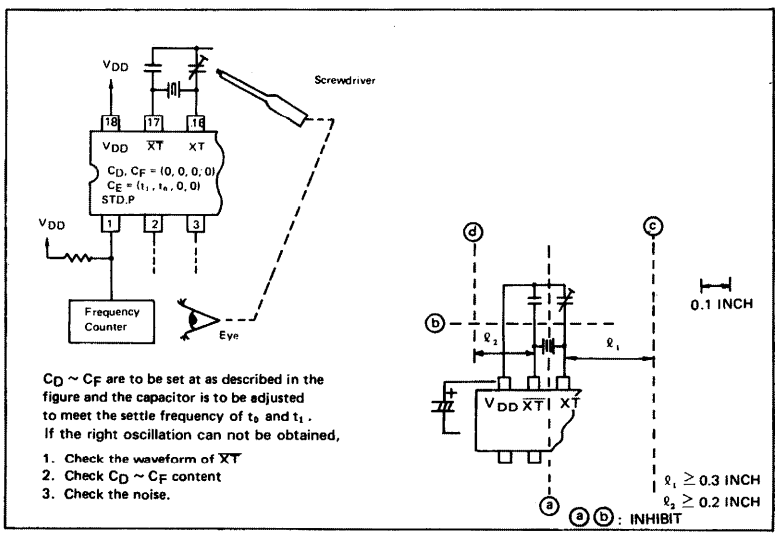
Figure 18.

APPLICATION NOTE

1. Power Supply



2. Adjustment of Frequency



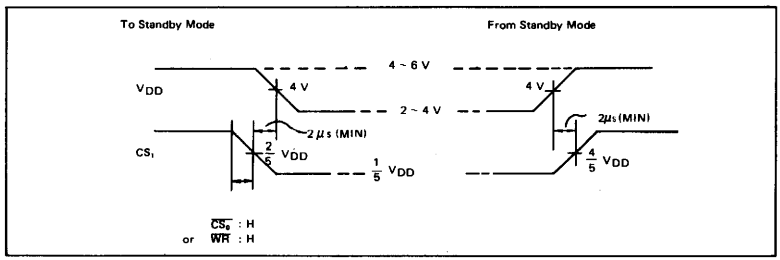
3. CH_1 (Chip Select)

V_{IH} and V_{IL} of CH_1 has 3 functions.

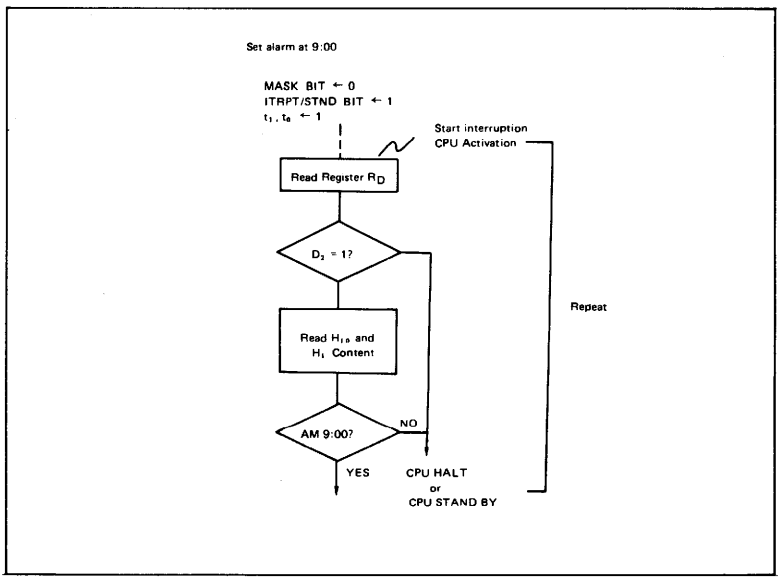
a) To accomplish the interface with a microcontroller/microprocessor.
b) To inhibit the control bus, data bus and address bus and to reduce input gate pass current in the stand-by mode.
c) To protect internal data when the mode is moved to and from standby mode.

To realize the above functions:

a) More than 4/5 V_{DD} should be applied to the MSM6242 for the interface with a microcontroller/microprocessor in 5V operation.
b) In moving to the standby mode, 1/5 V_{DD} should be applied so that all data buses should be disabled. In the standby mode, approx. 0V should be applied.
c) To and from the standby mode, obey following Timing chart.



4. Set STD.P at arlarm mode



TYPICAL APPLICATION – POWER SUPPLY CIRCUIT

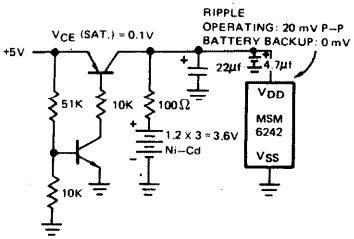


Figure 19.

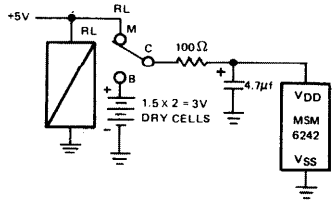


Figure 20.

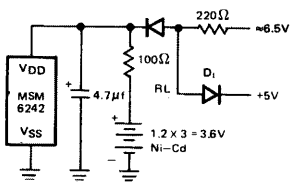
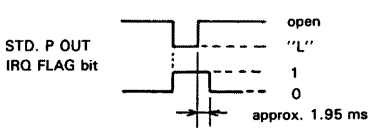


Figure 21.

4.7 μF: tantalum

SUPPLEMENTARY DESCRIPTION

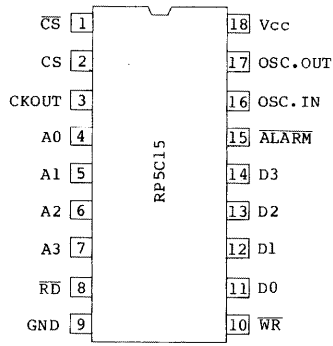
- When "0" is written to the IRQ FLAG bit, the IRQ FLAG bit is cleared. However, if "0" is assigned to the IRQ FLAG bit when written to the other bits, the 30-sec ADJ bit and the HOLD bit, the IRQ FLAG = 1 and was generated before the writing and IRQ FLG = 1 generated in a moment then will be cleared. To avoid this, always set "1" to the IRQ FLAG unless "0" is written to it intentionally. By writing "1" to it, the IRQ FLAG bit does not become "1".
- Since the IRQ FLAG bit becomes "1" in some cases when rewriting either of the t_1, t_0, or ITRPT/STND bit of register C_E, be sure to write "0" to the IRQ FLAG bit after writing to make valid the IRQ FLAG = 1 to be generated after it.
- The relationship between SDT. P OUT and IRQ FLAG bit is shown below:



Specifications of RP5C15

Outline:

The RP5C15 is a real-time clock that can be connected directly to the bus of microprocessors using not only the 8-bit CPU such as 8085, Z80, 6809, 6502 but also the 16-bit CPU such as 8086, Z8000, 68000 or others. Time can then be written to or read from the clock in the same way as writing to or reading from RAM. As well as calendar and time counters and alarm function allowing battery backup.

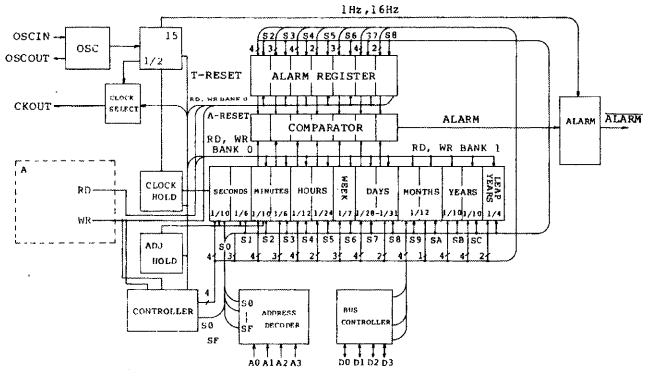


Pin configuration

Featrues:

* Direct connection to CPU and Hi-speed access
* 4-bit bidirectional bus D0~D3
* 4-bit address inputs A0~A3
* Internal counters for time (hours, min., sec.) and date (100 years, leap years, months, days, and days-of-the-week)
* All clock data expressed in BCD code
* ±30 sec. adjustment function
* Provision for battery backup
* Choice of standard clock from 16 kHz, 1.024 kHz, 128 kHz, 16 Hz, 1 Hz, 1/60 Hz
* Alarm signal, 16 Hz clock signal or 1 Hz clock signal output

Block diagram



Absolute maximum ratings (See Note 1)

Symbol	Item	Measurement conditions	Values	Units
VCC	Supply voltage	GND = 0	-0.3 ~ +7	V
VI	Input voltage	GND = 0	-0.3 ~ VCC+0.3	V
VC	Output voltage	GND = 0	-0.3 ~ VCC+0.3	V
PD	Maximum power dissipation	Ta = 25°C	600	mW
TOPG	Ambient temp. during operation		-20 ~ 70	°C
TSTG	Ambient temp. during storage		-40 ~ 125	°C

(Note 1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended operating conditions

Ta = -20°C to 70°C unless otherwise specified.

Symbol	Item	Values			Units
		Min.	Typ.	Max.	
VCC	Supply voltage	4.5	5.0	5.5	V
VDH	Data backup voltage	2.0		5.5	V
fxt	Oscillation frequency of crystal oscillator		32.768		kHz

DC characteristics during normal operation

Ta = -20°C to 70°C, Vcc = 5V ±10% unless otherwise specified.

Symbol	Item	Measurement conditions	Values			Units	Remarks
			Min.	Typ.	Max.		
VIH	"H" input voltage		2.0		Vcc+0.3	V	
VIL	"L" input voltage		-0.3		0.8	V	
VOH	"H" output voltage	IOH=-400μA	2.4			V	Except for pin 3,15
VOL	"L" output voltage	IOL=2mA			0.4	V	
IILK	Input leakage current	VIN=0 ~ VCC	-10		10	μA	
IFLK	Floating leakage current	VFV=0 ~ VCC	-10		10	μA	
IDDI	Current consumed during operation	(Note 2)			300	μA	

(Note 2) Vcc = 5V; R/W signal f =100kHz; Input terminals, Vcc or GND; Output terminals on no-load; Crystal oscillator (32.768kHz); Measurement temp. (25°C).

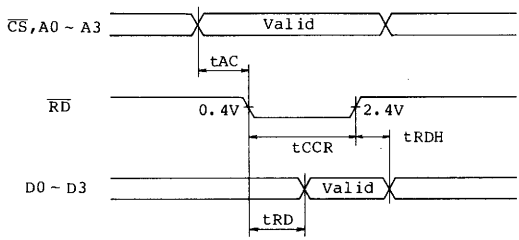
AC electrical characteristics

Ta=-20°C to 70°C, Vcc=5V±10% unless otherwise specified.

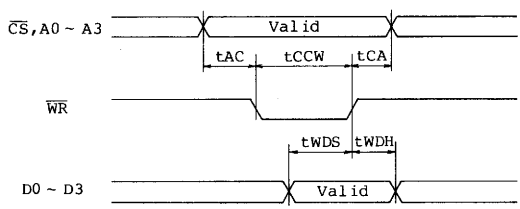
Symbol	Item	Measurement conditions	Values			Units	Remarks
			Min.	Typ.	Max.		
tAC	Address valid -- $\overline{RD}/\overline{WR}$ trailing edge		50			ns	$\overline{CS}$=low and address valid
tccR	$\overline{RD}$ pulse width		120		13000	ns	
tccW	$\overline{WR}$ pulse width		120		13000	ns	
tRD	$\overline{RD}$ trailing edge --data valid	(Note 1)			120	ns	
tcA	$\overline{RD}/\overline{WR}$ leading edge --address hold		10			ns	
tWDS	Write data setup time		100			ns	
tWDH	Write data hold time		20			ns	
tRDH	$\overline{RD}$ leading edge --data valid		10			ns	
tEN-DIS	Timer Enable-- Timer Disable		100			μs	
tADJ	Adjustment completion time				100	μs	
tAINH	Alarm data write inhibit time after alarm reset		100			μs	
tRCV	$\overline{RD}/\overline{WR}$ recovery time		1			μs	

Timing chart

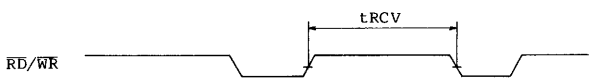
READ cycle (CS = "H")



WRITE cycle (CS = "H")



Others



Function of pins

Name of pin	No. of pin	Function
$\overline{CS}$ CS	1 2	External interface terminals. Valid when both CS = H and $\overline{CS}$ = L. CS is connected to the power-down detector of the peripheral circuitry, and $\overline{CS}$ to the address decoder of the CPU.
CKOUT	3	Output terminal for standard clock signal. Can take 8 different states depending on contents of CKOUT selection register. N-ch open drain output.
A0 ~ A3	4,5,6,7	Address input. Connected to address bus of CPU.
$\overline{RD}$	8	I/O control input. Set to low when data of RP5C15 is read. Low active input.
GND	9	OV
$\overline{WR}$	10	I/O control input. Set to low when data of RP5C15 is written. Low active input.
D0 ~ D3	11,12,13,14	Bidirectional bus. Connected directly to CPU data bus.
$\overline{ALARM}$	15	Output terminal for alarm signal and 1Hz/16Hz clock signals. N-ch open-drain output.
OSC IN	16	Connected to 32.768kHz crystal oscillator circuit.
OSC OUT	17	Connected to 32.768kHz crystal oscillator circuit.
VCC	18	+5V power supply

Address allocation

* "x" means "Don't care" when written, and always "0" when read out.
* Address 0~D: able to read to and write from, except for ADJUST register which can only be written to.
  Address E~F: "write" only (always "0" when read out)

Bank 0						Bank 1				
A_3~A_0	Contents	D_3	D_2	D_1	D_0	Contents	D_3	D_2	D_1	D_0
0	1-sec. counter					CKOUT selection register	X	CK2	CK1	CK0
1	10-sec. counter	X				Adjust register	X	X	X	Adjust
2	1-min. counter					Alarm 1-min. register				
3	10-min. counter	X				Alarm 10-min. register	X			
4	1-hour counter					Alarm 1-hour register				
5	10-hour counter	X	X			Alarm 10-hour register	X	X		
6	Day-of-the-week counter	X				Alarm day-of-the-week register	X			
7	1-day counter					Alarm 1-day register				
8	10-day counter	X	X			Alarm 10-day register	X	X		
9	1-month counter						X	X	X	X
A	10-month counter	X	X	X		$\overline{12}$/24 hour selector	X	X	X	
B	1-year counter					Leap-year counter	X	X		
C	10-year counter						X	X	X	X
D	Mode register	Timer EN	Alarm EN	X	Bank 1/0	Mode register	Timer EN	Alarm EN	X	Bank 1/0
E	Test register	Test 3	Test 2	Test 1	Test 0	Test register	Test 3	Test 2	Test 1	Test 0
F	Reset controller	$\overline{1Hz}$ $\overline{ON}$	$\overline{16Hz}$ $\overline{ON}$	Timer RESET	Alarm RESET	Reset controller	$\overline{1Hz}$ $\overline{ON}$	$\overline{16Hz}$ $\overline{ON}$	Timer RESET	Alarm RESET

CKOUT selection register

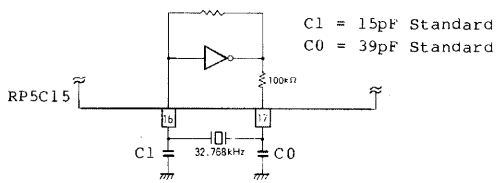
D3	D2	D1	D0	CKOUT	Remarks
X	0	0	0	"Z"	High-impedance
X	0	0	1	16.384kHz	Duty 50%
X	0	1	0	1.024kHz	Duty 50%
X	0	1	1	128Hz	Duty 50%
X	1	0	0	16Hz	Duty 50%
X	1	0	1	1Hz	↓Seconds counter increment. Duty 50%
X	1	1	0	1/60Hz	↓Minutes counter increment. Duty 50%
X	1	1	1	"L"	Low Level

Adjustment function

BANK 1 ADDRESS (A3,A2,A1,A0)=(0,0,0,1) DATA (D3,D2,D1,D0)=(X,X,X,1)	Second counter backs to 0 when it's adjusted 0 ~ 29 sec. If it's adjusted on 30 ~ 59 sec., the second counter goes up to 0 sec. and the minute counter shows the next minute.

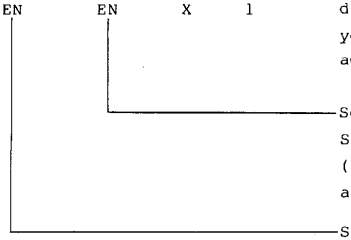
Oscillator circuit

Not required because an output ballast registor (Approx. 100kΩ) is used.



*Bank register (A3,A2,A1,A0) = (1,1,0,1) = D

D3	D2	D1	D0	
Timer EN	Alarm EN	X	0	BANK0:setting or rate time
		X	1	BANK1:setting or rate of Alarm data, 12/24 hour system, leap year, choice of CLKOUT, and adjustment



Set 1 to enable alarm output
Set 0 to disable alarm output
(16Hz/1Hz clock signals not affected)

Set 1 to start clock. Set 0 to stop seconds and subsequent counters.

*The leap-year counter registers a leap year when D1 = D0 = 0. It simultaneously counts with the year counter.

*The 12-hour/24-hour selector sets the 12-hour system when D0 = 0 and the 24-hour system when D0 = 1. PM or AM is selected when D1 in the 10-hour counter is 1 or 0, respectively.

*Reset controller 16Hz/1Hz clock register.

(A3,A2,A1,A0) = (1,1,1,1) = F

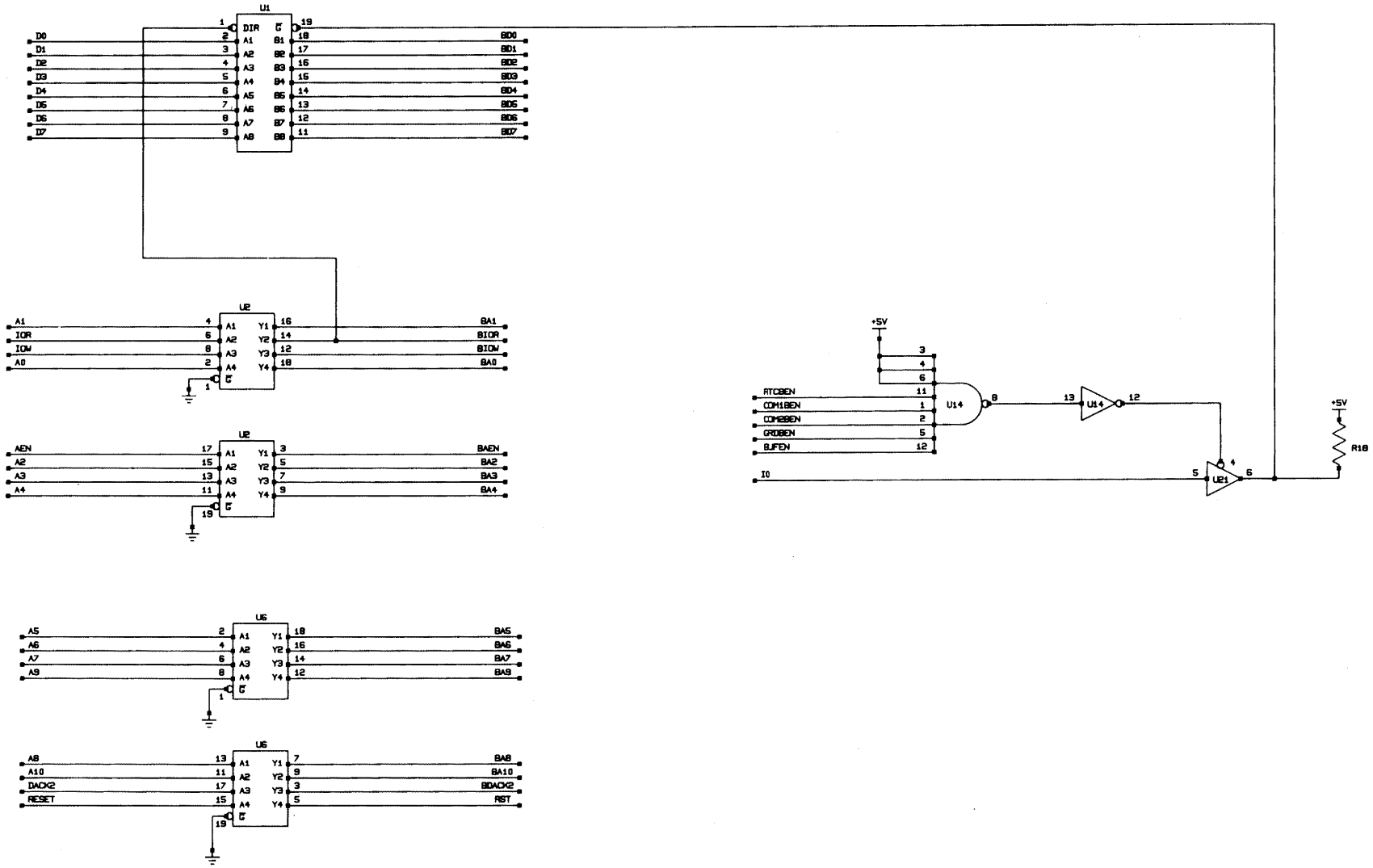
D0 = 1:resets all alarm register and internal Alarm F/Fs.
D1 = 1:dividers before seconds counter reset.
D2 = 0:switches on the 16Hz clock pulse generated from the ALARM terminal.
D3 = 0:switches on the 1Hz clock pulse generated from the ALARM terminal.

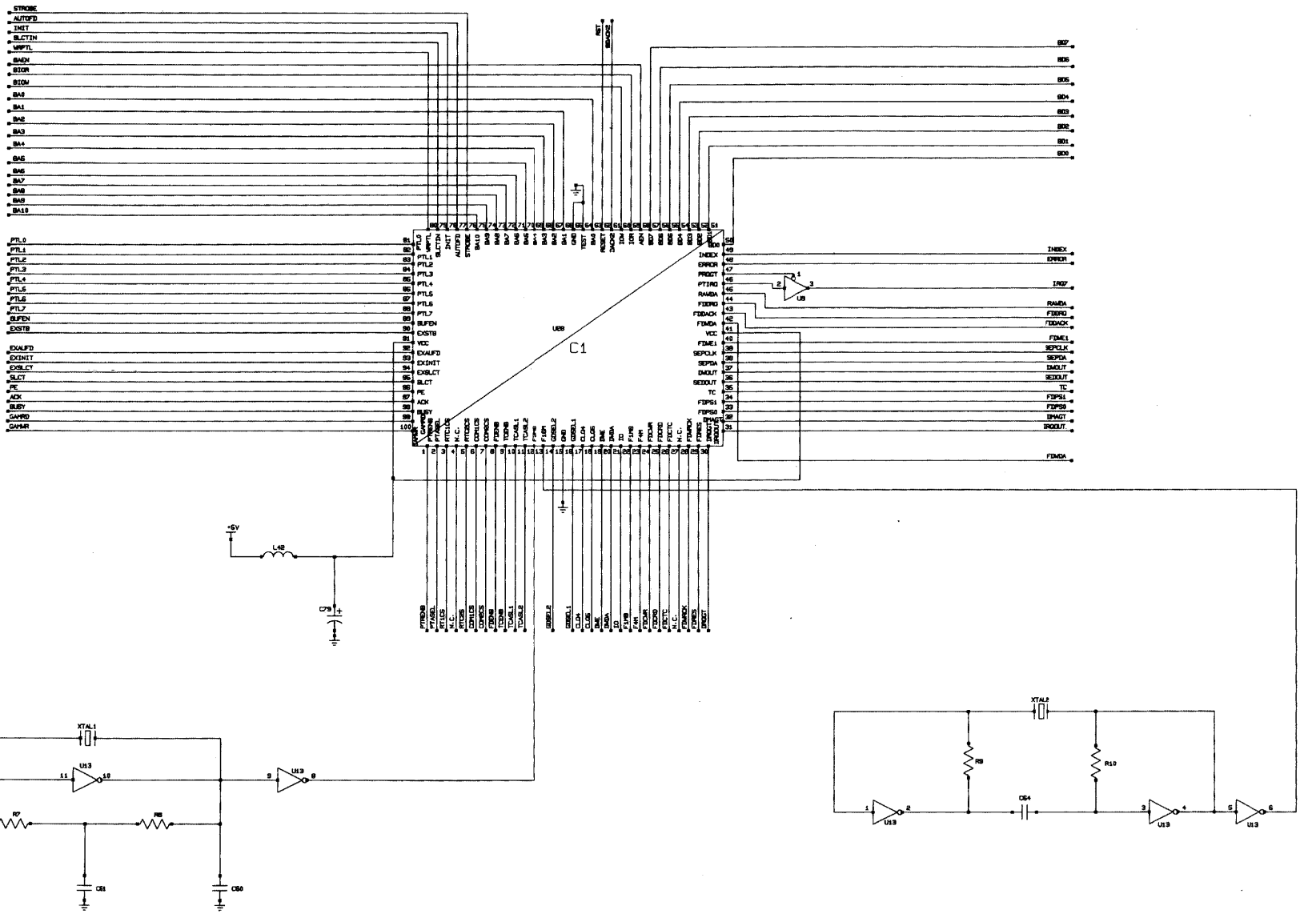
*Addresses 0 ~ D:able to read and write.

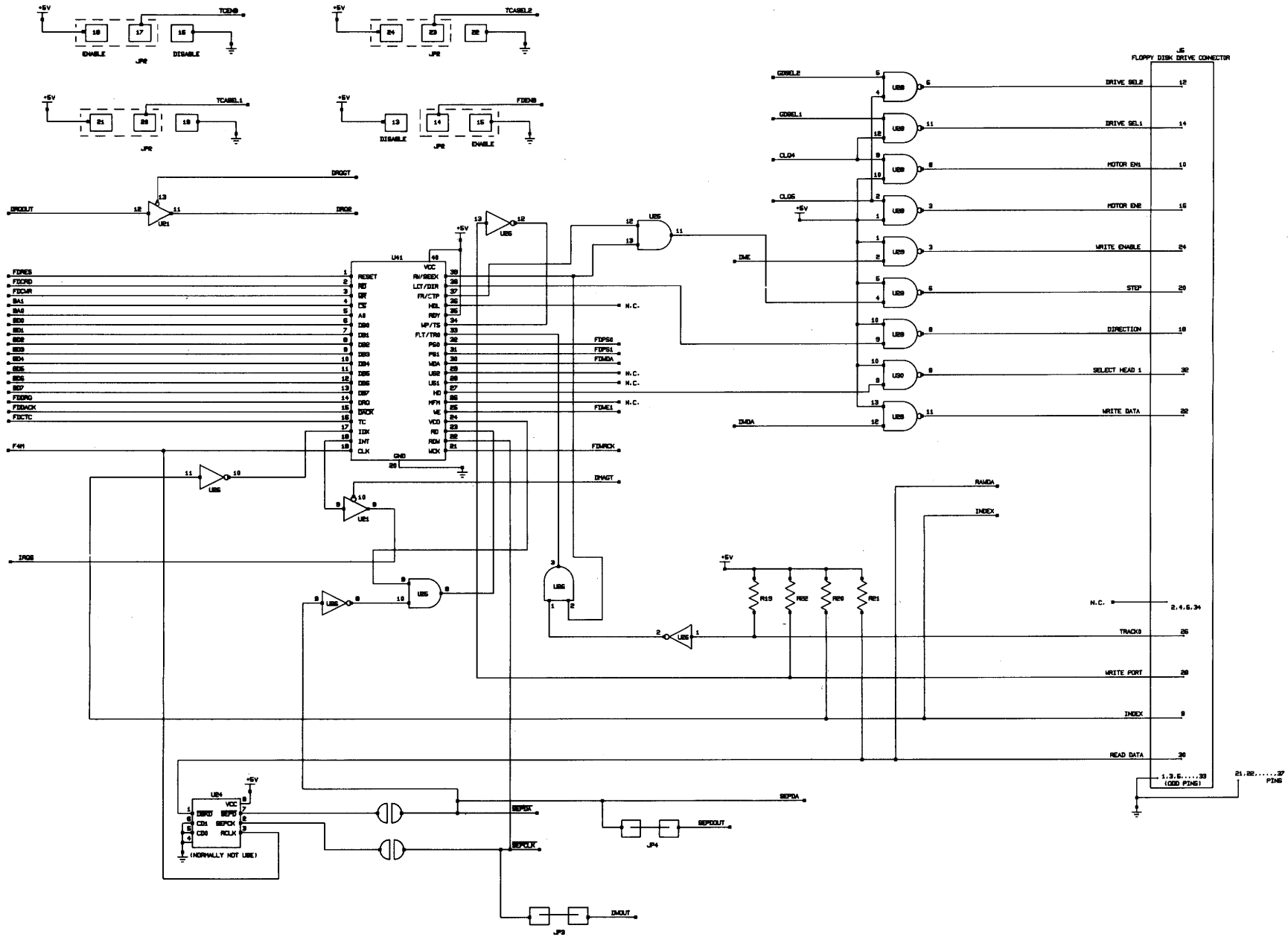
*Addresses E ~ F:only able to write and 0H always appears when read out.

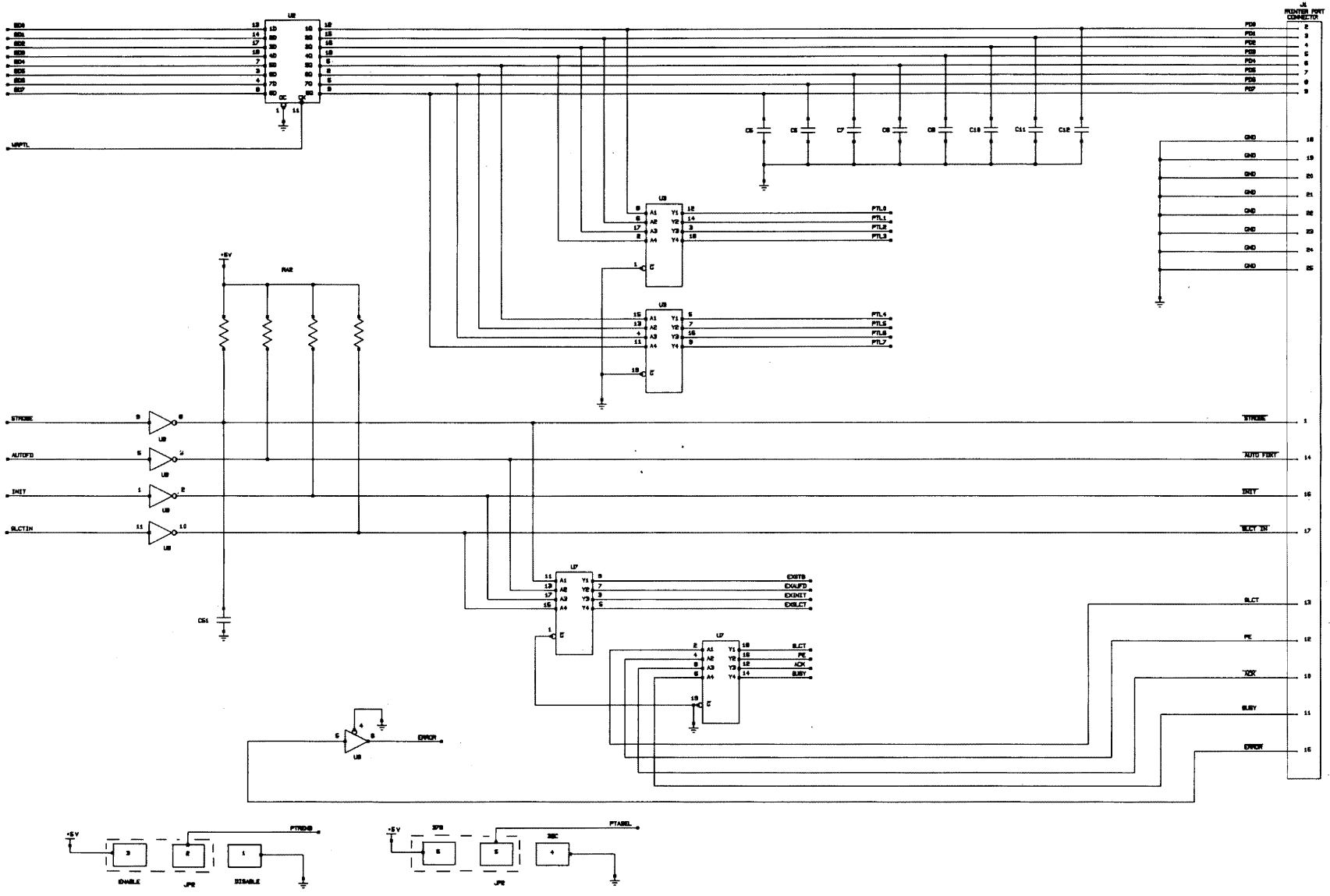
*TEST register (A3,A2,A1,A0) = (1,1,1,0) = E:use for inspections at Ricoh Co., Ltd. Normal watch function is achieved by setting of the data (D3,D2,D1,D0) = (0,0,0,0).

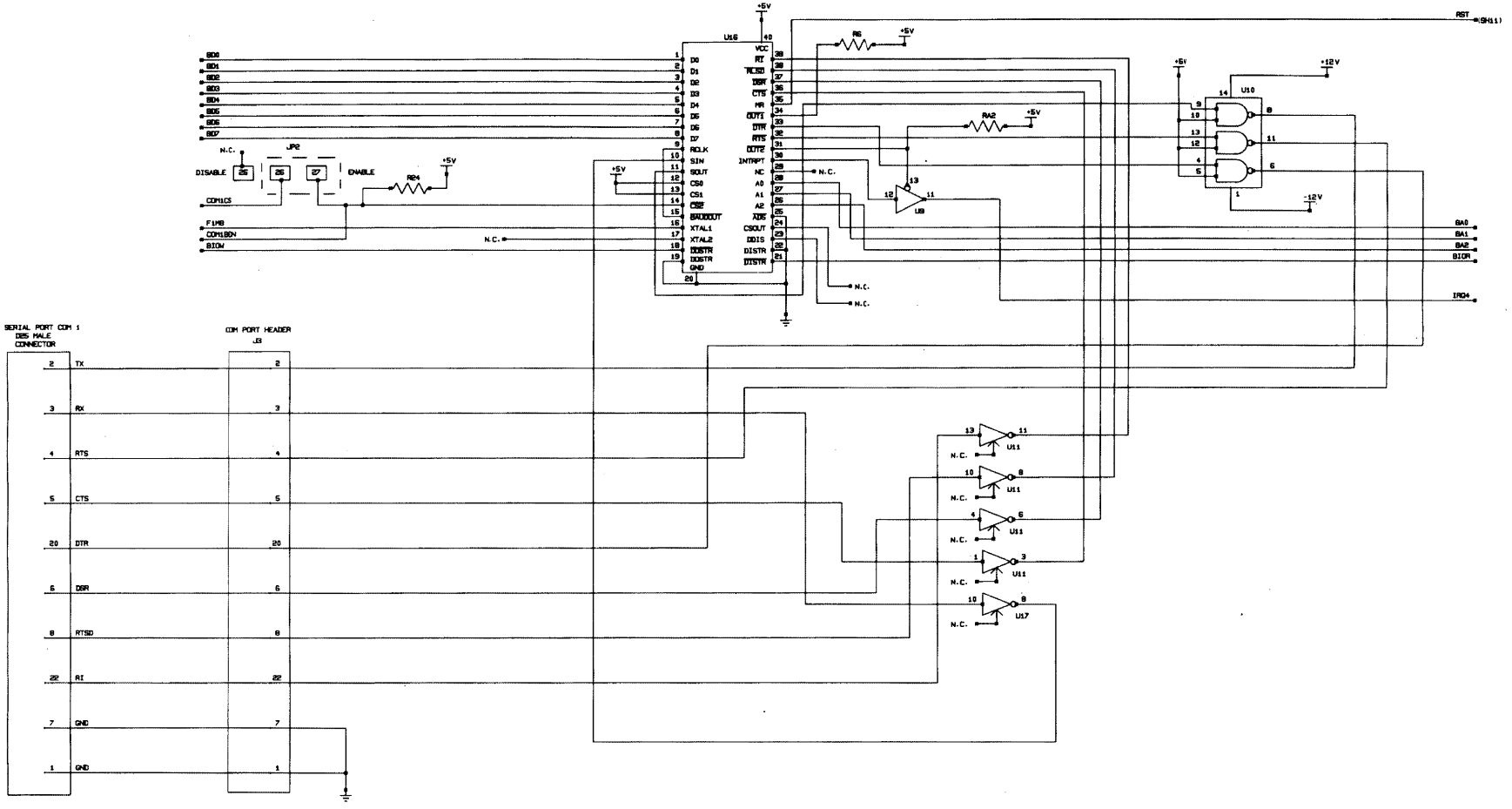
For details, refer to the Application Manual.

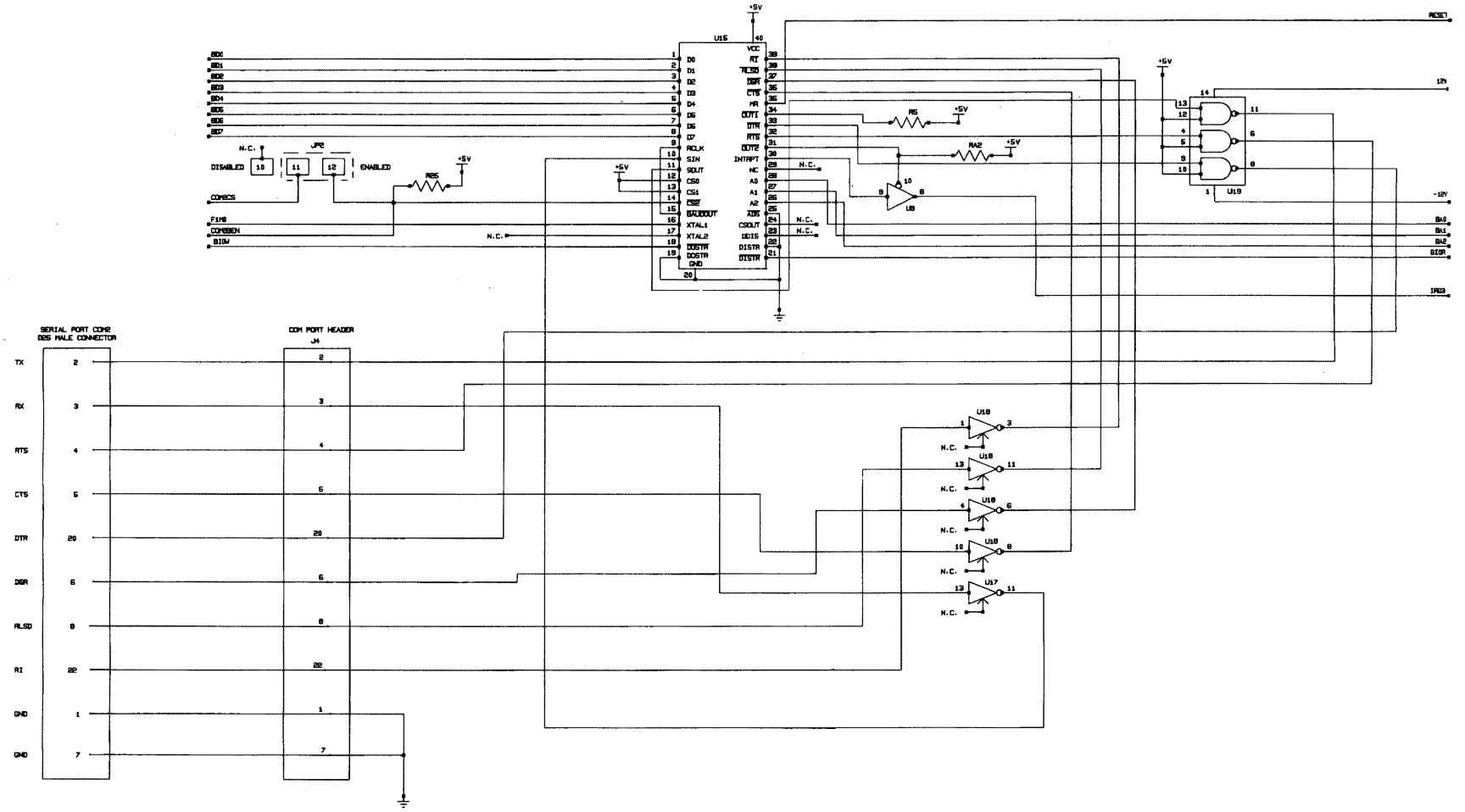

U1
DIR
D0
D1
D2
D3
D4
D5
D6
D7
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
U2
A1
IOR
IOW
A0
BA1
BIOR
BIOW
BA0
U2
AEN
A2
A3
A4
BAEN
BA2
BA3
BA4
U6
A5
A6
A7
A9
BA5
BA6
BA7
BA9
U6
A8
A10
DACK2
RESET
BA8
BA10
BDACK2
RST
+5V
RTCBEN
COM1BEN
COM2BEN
GRDBEN
BUFEN
U14
U14
+5V
R18
IO
U21

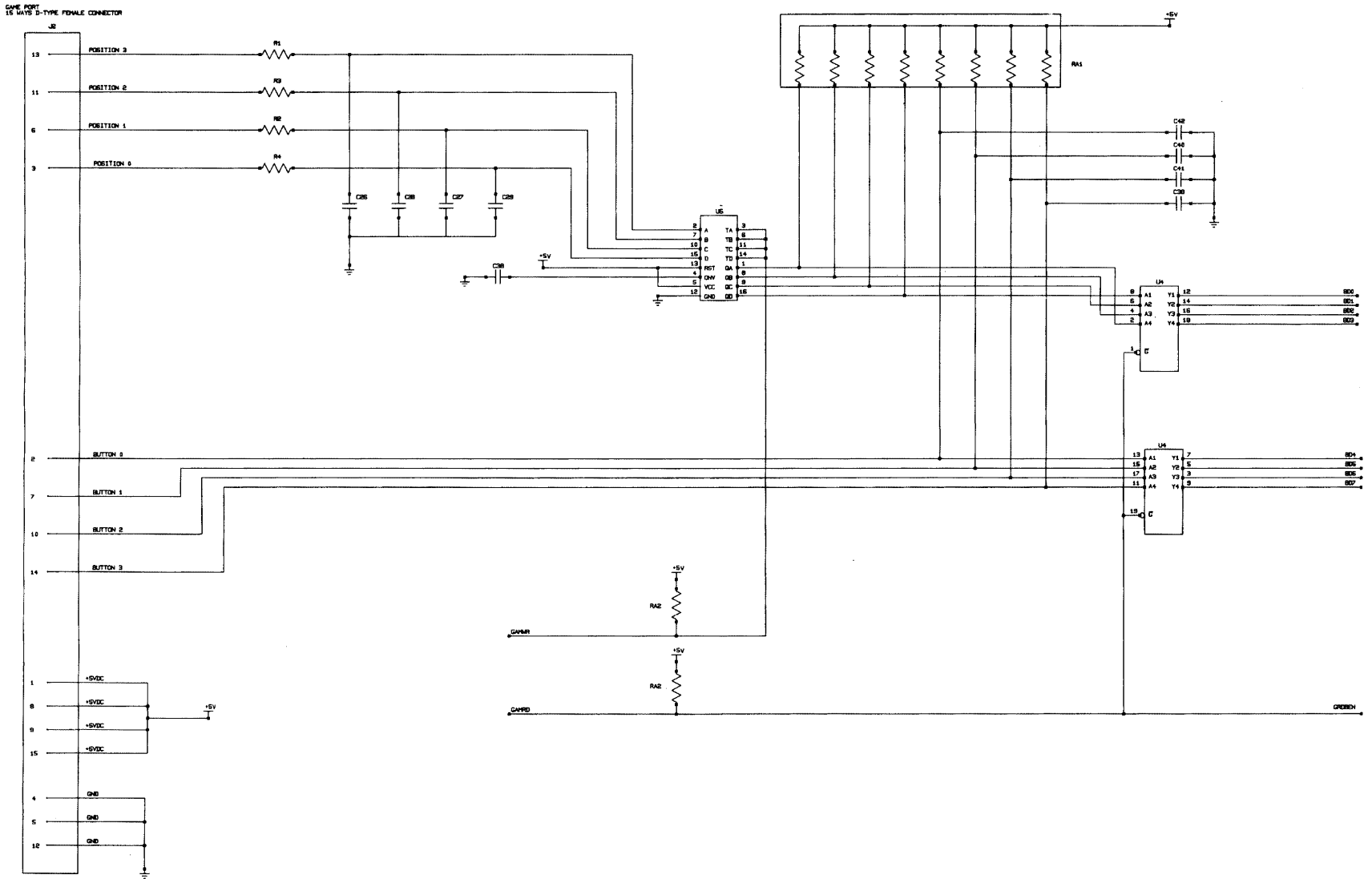

STROBE
AUTOFD
INIT
SLCTIN
WRPTL
BAEN
BIOR
BIOW
BA0
BA1
BA2
BA3
BA4
BA5
BA6
BA7
BA8
BA9
BA10
PTL0
PTL1
PTL2
PTL3
PTL4
PTL5
PTL6
PTL7
BUFEN
EXSTB
EXAUFD
EXINIT
EXSLCT
SLCT
PE
ACK
BUSY
GAMRD
GAMWR
RST
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BD0
INDEX
ERROR
IRQ7
RAMDA
FDDRQ
FDDACK
FDMDA
FDME1
SEPCLK
SEPDA
DMOUT
SEDOUT
TC
FDPS1
FDPS0
IRQGT
IRQOUT
U69
C1
+5V
L48
C79
XTAL1
U13
R7
R8
C82
C81
C80
XTAL2
R9
R10
C84

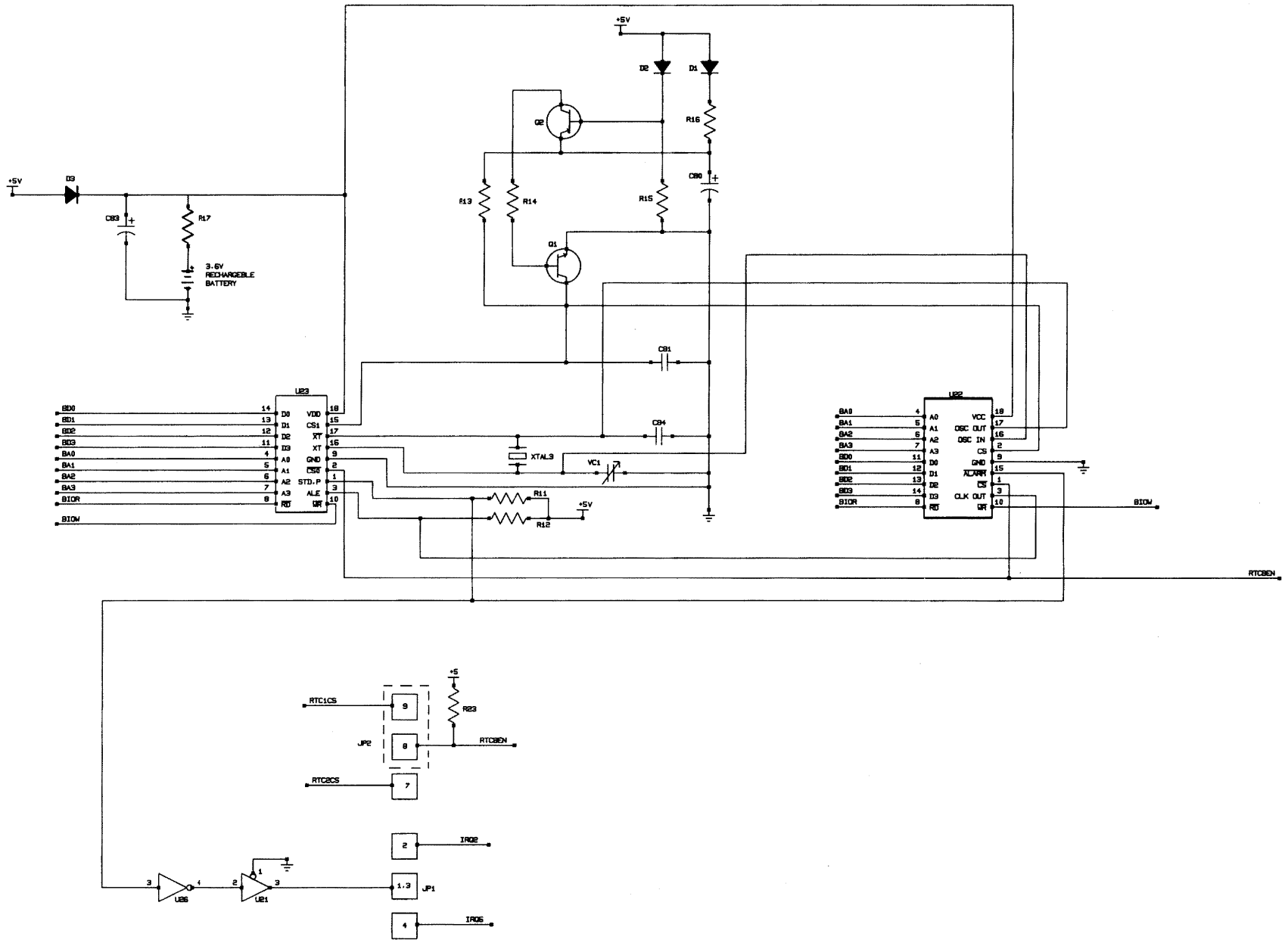

+5V
TCEN0
ENABLE
DISABLE
JP2
TCABEL2
TCABEL1
FDEN0
DISABLE
ENABLE
DRQOUT
DRQIN
U41
RESET
RD
WR
CS
A0
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DRQ
DACK
TC
IDX
INT
CLK
VCC
RW/SEEK
LCT/DIR
FR/CTP
HDL
RDY
WP/TS
FLT/TRK0
PS0
PS1
WDA
WG
WE
VCC
RD
RDW
WCK
GND
FDRES
FDCRD
FDCWR
DA1
DA0
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
FDDRQ
FDDACK
FDCTC
F4M
IRQ6
FDPS0
FDPS1
FDWDA
FDWE1
FDWRCK
DMAGT
N.C.
U26
U27
U28
U29
U30
U31
U32
U33
U34
U35
U36
U37
U38
U39
U40
GDSEL2
GDSEL1
CLD4
CLD5
DME
DMDA
RAWDA
INDEX
SEPDA
SEPCLK
SEPDOUT
DMOUT
JP3
JP4
R19
R22
R20
R21
J5
FLOPPY DISK DRIVE CONNECTOR
DRIVE SEL2
DRIVE SEL1
MOTOR EN1
MOTOR EN2
WRITE ENABLE
STEP
DIRECTION
SELECT HEAD 1
WRITE DATA
TRACK0
WRITE PORT
INDEX
READ DATA
2,4,6,34
1,3,5.....33
(ODD PINS)
21,22.....37
PINS
U24
VCC
INRQ
SEPDT
CD1
SEPCK
CD0
RCLK
(NORMALLY NOT USE)

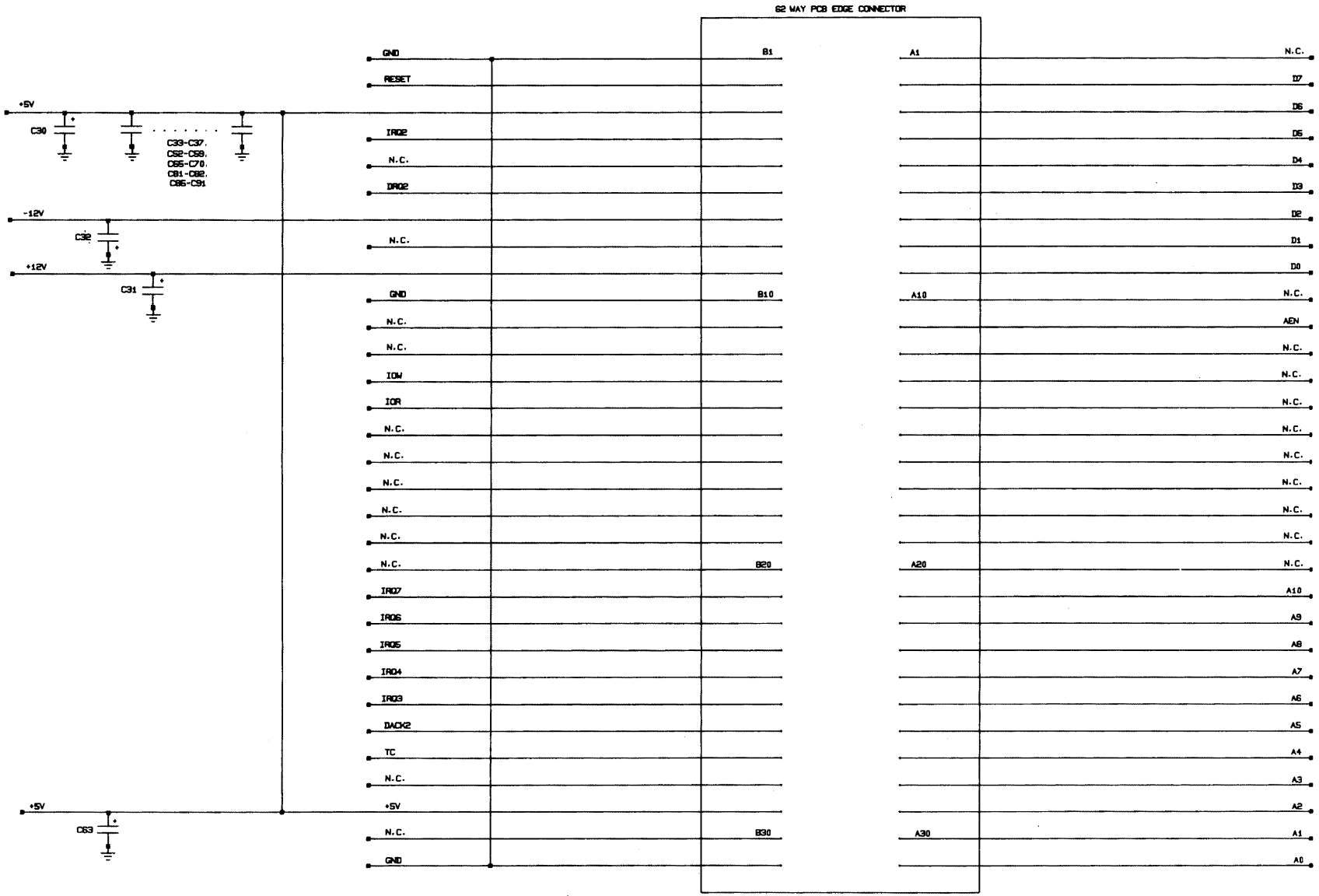

PRINTER PORT CONNECTOR
STROBE
AUTOFD
INIT
SLCTIN
ERROR
PTRDIS
PTABEL
ENABLE
DISABLE
JPR

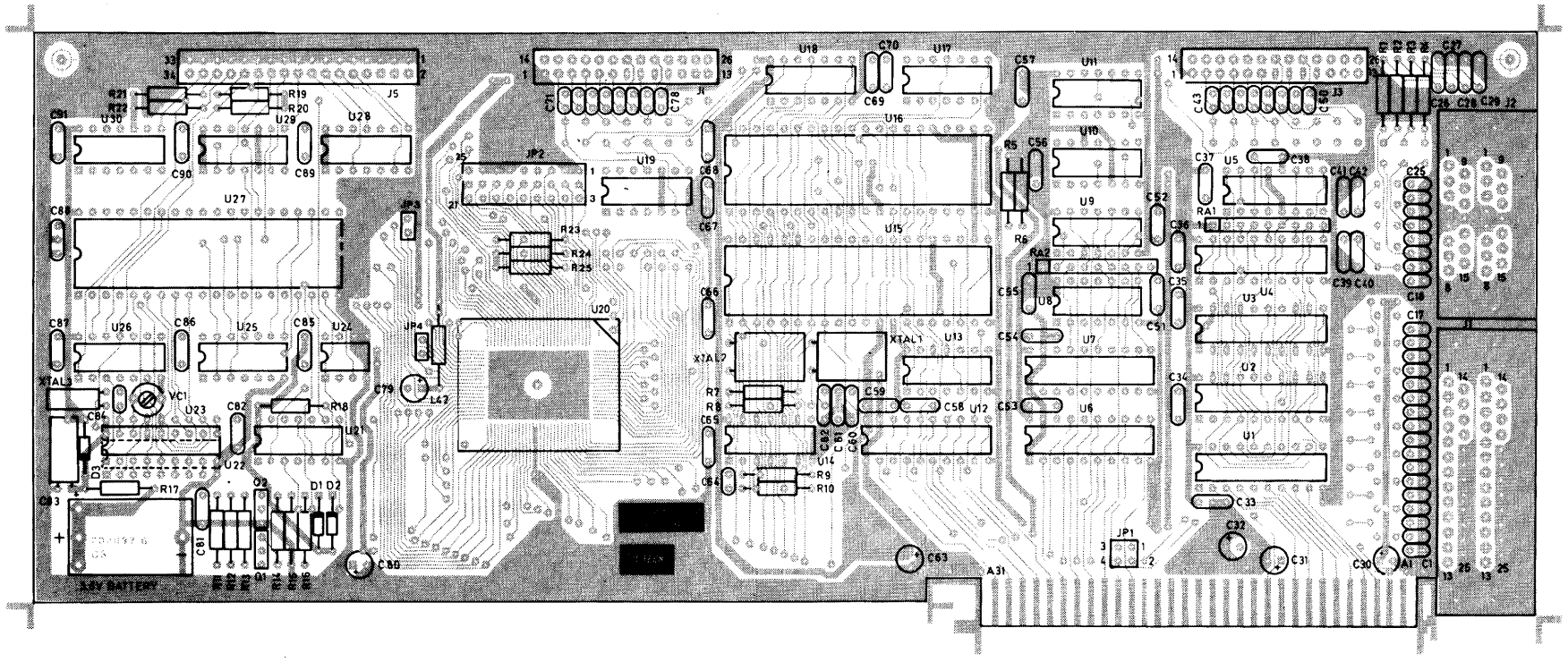

SERIAL PORT COM 1
DB9 MALE
CONNECTOR
COM PORT HEADER
J3
TX
RX
RTS
CTS
DTR
DSR
RTSD
RI
GND
GND
U16
JP2
DISABLE
ENABLE
COM1CS
FIMB
COM1BN
BIOW
RP4
RP6
RA2
U10
U9
U11
U17
RST
BA0
BA1
BA2
BIOR
IRQ4
N.C.
+5V
+12V
-12V

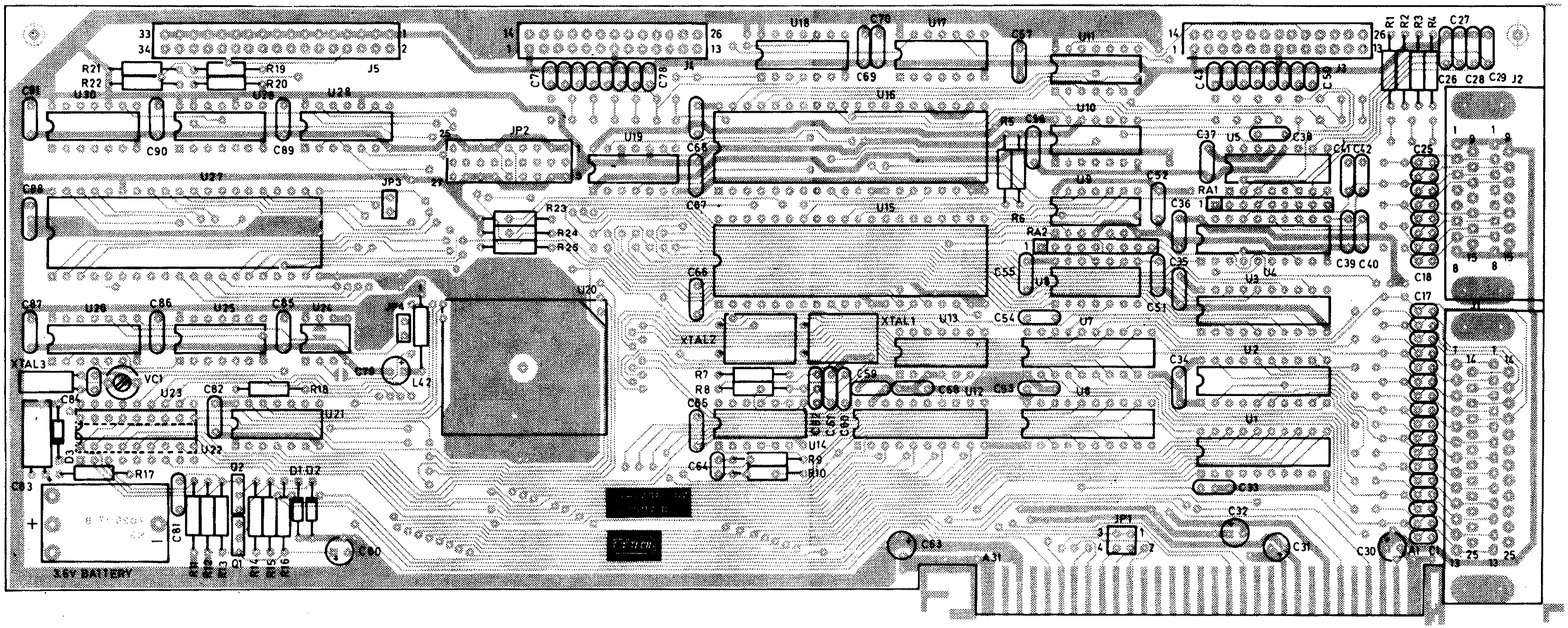

SERIAL PORT COM2
DB9 MALE CONNECTOR
COM PORT HEADER
J4
TX
RX
RTS
CTS
DTR
DSR
RLSD
RI
GND
GND
U15
D0
D1
D2
D3
D4
D5
D6
D7
RCLK
SIN
SOUT
CS0
CS1
CS2
BAUDOUT
XTAL1
XTAL2
DOSTR
DOSTR
GND
VCC
RI
RLSD
DSR
CTS
MR
OUT1
DTR
RTS
OUT2
INTRPT
NC
A0
A1
A2
ADS
CSOUT
DDIS
DISTR
DISTR
+5V
JP2
DISABLED
ENABLED
COM2CS
FIN8
COM8EN
8IOW
R25
R5
RA2
N.C.
RESET
12V
-12V
BA0
BA1
BA2
8IOR
IRQ8
U16
U17
U18
U19


GAME PORT
15 WAYS D-TYPE FEMALE CONNECTOR
J2
POSITION 3
POSITION 2
POSITION 1
POSITION 0
R1
R3
R2
R4
C25
C26
C27
C28
C30
U5
RA1
C42
C40
C41
C39
U4
BD0
BD1
BD2
BD3
BUTTON 0
BUTTON 1
BUTTON 2
BUTTON 3
+5VDC
GND
RA2
GAMBR
GAMBD
GREEN


+5V
D3
CB3
R17
3.6V
RECHARGEBLE
BATTERY
D2
D1
Q2
R16
CB0
R13
R14
R15
Q1
CB1
CB4
XTAL3
VC1
R11
R12
+5V
U23
BD0
BD1
BD2
BD3
BA0
BA1
BA2
BA3
BIOR
BIOW
D0
D1
D2
D3
A0
A1
A2
A3
RD
VDD
CS1
XT
XT
GND
CS0
STD.P
ALE
WR
U22
BA0
BA1
BA2
BA3
BD0
BD1
BD2
BD3
BIOR
A0
A1
A2
A3
D0
D1
D2
D3
RD
VCC
OSC OUT
OSC IN
CS
GND
ALARM
CS
CLK OUT
WR
BIOW
RTCBEN
RTC1CS
JP2
R23
RTCBEN
RTC2CS
IRQ2
JP1
IRQ6
U86
U21


62 WAY PCB EDGE CONNECTOR
+5V
C30
C33-C37,
C52-C59,
C65-C70,
C81-C82,
C85-C91
-12V
C32
+12V
C31
+5V
C63
GND
RESET
IRQ2
N.C.
DRQ2
N.C.
GND
N.C.
N.C.
IOW
IOR
N.C.
N.C.
N.C.
N.C.
N.C.
N.C.
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
DACK2
TC
N.C.
+5V
N.C.
GND
B1
B10
B20
B30
A1
A10
A20
A30
N.C.
D7
D6
D5
D4
D3
D2
D1
D0
N.C.
AEN
N.C.
N.C.
N.C.
N.C.
N.C.
N.C.
N.C.
N.C.
N.C.
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0


J5
J4
J3
J2
J1
JP1
JP2
JP3
JP4
U30
U29
U28
U27
U26
U25
U24
U23
U22
U21
U20
U19
U18
U17
U16
U15
U14
U13
U12
U11
U10
U9
U8
U7
U6
U5
U4
U3
U2
U1
XTAL1
XTAL2
VC1
L42
A31
3.6V BATTERY


J5
J4
J3
J2
U30
U29
U28
U27
U26
U25
U24
U23
U22
U21
U20
U19
U18
U17
U16
U15
U14
U13
U12
U11
U10
U9
U8
U7
U6
U5
U4
U3
U2
U1
JP1
JP2
JP3
JP4
XTAL1
XTAL2
XTAL3
VC1
L42
RA1
RA2
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R17
R18
R19
R20
R21
R22
R23
R24
R25
C17
C18
C25
C26
C27
C28
C29
C30
C31
C32
C33
C34
C35
C36
C37
C38
C39
C40
C41
C42
C51
C52
C53
C54
C55
C56
C57
C59
C60
C63
C64
C65
C66
C67
C68
C69
C70
C79
C80
C81
C82
C83
C84
C85
C86
C87
C88
C89
C90
C91
D1
D2
D3
Q1
Q2
A1
A31
3.6V BATTERY

LASER MULTI-I/O CARD (G/A) COMPONENT LOCATION LIST

DESTINATION	PART NUMBER	DESCRIPTION
J2	40-0388-15-02	D15 FEMALE CONNECTOR(PCB TYPE)
J1	40-0388-25-02	D25 FEMALE CONNECTOR(PCB TYPE)
JP1	40-0184-00-01	WAFER 2 PINS (CPI)
	v40-0184-00-00	WAFER 2 PINS (MOLEX)
JP2	40-0215-00-01	WAFER 3 PINS (CPI)
	v40-0215-00-00	WAFER 3 PINS (MOLEX)
J3,J4	40-0194-00-01	WAFER 13 PINS (CPI)
	v40-0194-00-00	WAFER 13 PINS (MOLEX)
J5	40-0194-00-01	WAFER 13 PINS (CPI)
	v40-0194-00-00	WAFER 13 PINS (MOLEX)
AND	40-0216-00-01	WAFER 4 PINS (CPI)
	v40-0216-00-00	WAFER 4 PINS (MOLEX)
U20	27-0604-00-00	GATE ARRAY C1
U18	40-0283-01-01	I.C. SOCKET 14 PINS (FOR 1488)
U19	40-0283-01-01	I.C. SOCKET 14 PINS (FOR 1489)
U27	27-0525-00-02	I.C. FDC (ZILOG) Z765A08PSC
	v27-0525-00-00	I.C. FDC (NEC) UPD765AC
	v27-0525-00-01	I.C. FDC (ROCKWELL) UPD765A
U16	27-0365-00-00	I.C. IN8250 (N.S.)
	v27-0365-00-01	I.C. WD8250 (WESTERN)
U15	40-0008-00-03	I.C. SOCKET 40 PINS FOR IN8250
	v40-0008-00-00	I.C. SOCKET 40 PINS FOR IN8250
U23	27-0619-01-00	RTC MSM6242BRS (OKI)
	a27-0619-00-00	RTC MSM6242RS (OKI)
OR	27-0498-00-00	RP5C15 (USE U22 LOCATION)
U5	27-0201-00-02	QUAD TIMER XR-558 (EXAR)
	v27-0201-00-01	I.C. NE558 (SIGNETICS)
U10	27-0363-00-05	XR1488 (EXAR)
	v27-0363-00-00	MC1488 (MOTOROLA)
	v27-0363-00-01	MC1488 (TEXAS)
	v27-0363-00-02	MC1488 (SIGNETICS)
U11,U17	27-0364-00-05	XR1489 (EXAR)
	v27-0364-00-00	MC1489 (MOTOROLA)
	v27-0364-00-02	MC1489 (SIGNETICS)
U2	27-0195-00-00	I.C. 74LS374 (MOTOROLA)
	v27-0195-00-01	I.C. 74LS374 (T.I.)
	v27-0195-00-02	I.C. 74LS374 (HITACHI)
	v27-0195-00-03	I.C. 74LS374 (FAIRCHILD)
U1	27-0100-00-01	I.C. 74LS245 (MOTOROLA)
	v27-0100-00-02	I.C. 74LS245 (FAIRCHILD)
	v27-0100-00-03	I.C. 74LS245 (HITACHI)
	v27-0100-00-04	I.C. 74LS245 (T.I.)
	v27-0100-00-05	I.C. 74LS245 (MITSUSIDER)
	v27-0100-00-06	I.C. 74LS245 (MATSUSHITA)
	v27-0100-00-07	I.C. 74LS245 (N.S.)

U3,U4,U6,	27-0160-00-00	I.C. 74LS244 (MOTOROLA)
U7,U12	v27-0160-00-01	I.C. 74LS244 (FAIRCHILD)
	v27-0160-00-02	I.C. 74LS244 (HITACHI)
	v27-0160-00-03	I.C. 74LS244 (T.I.)
	v27-0160-00-04	I.C. 74LS244
	v27-0160-00-05	I.C. 74LS244 (MATSUSHITA)
	v27-0160-00-06	I.C. 74LS244 (N.S.)
	v27-0160-00-07	I.C. 74LS244 (SGS)
U14,U26	27-0038-02-00	I.C. 74LS04 (HITACHI)
	v27-0038-02-01	I.C. 74LS04 (SCISYS)
	v27-0038-02-02	I.C. 74LS04 (FAIRCHILD)
	v27-0038-02-03	I.C. 74LS04 (MOTOROLA)
	v27-0038-02-04	I.C. 74LS04 (N.S.)
	v27-0038-02-05	I.C. 74LS04
	v27-0038-02-06	I.C. 74LS04 (SGS)
	27-0057-00-02	I.C. 74LS05 (HITACHI)
	v27-0057-00-03	I.C. 74LS05 (TEXAS)
	v27-0057-00-01	I.C. 74LS05 (SCISYS)
	v27-0057-00-04	I.C. 74LS05 (N.S.)
	v27-0057-00-05	I.C. 74LS05 (MOTOROLA)
U25	27-0184-00-00	I.C. 74LS08 (HITACHI)
	v27-0184-00-01	I.C. 74LS08
	v27-0184-00-04	I.C. 74LS08 (TEXAS)
	v27-0184-00-05	I.C. 74LS08 (MOTOROLA)
	a27-0444-00-00	I.C. 74HCT08 (RCA)
U9,U21	27-0209-00-01	I.C. 74LS125 (HITACHI)
	v27-0209-00-00	I.C. 74LS125 (MOTOROLA)
	v27-0209-00-03	I.C. 74LS125 (TEXAS)
U13	27-0171-00-04	I.C. 74LS30 (HITACHI)
	v27-0171-00-00	I.C. 74LS30 (MOTOROLA)
	v27-0171-00-01	I.C. 74LS30 (FAIRCHILD)
	v27-0171-00-03	I.C. 74LS30 (TEXAS)
U28,U29,U30	27-0241-00-01	I.C. 7438 (TEXAS)
	v27-0241-00-00	I.C. 7438 (MOTOROLA)
RA1,RA2	26-1472-08-13	RESISTOR NETWORK 4K7x8,9 PINS
	v26-1472-08-00	RESISTOR NETWORK 4K7x8,9 PINS
	v26-1472-08-01	RESISTOR NETWORK 4K7x8,9 PINS
	v26-1472-08-02	RESISTOR NETWORK 4K7x8,9 PINS
	v26-1472-08-05	RESISTOR NETWORK 4K7x8,9 PINS
XTAL2	25-3026-00-03	CRYSTAL 16MHZ (IPL)
	v25-3026-00-00	CRYSTAL 16MHZ (NAKAGAWA)
XTAL3	25-3009-00-03	CRYSTAL 32.768KHZ (IPL)
	v25-3009-00-00	CRYSTAL 32.768KHZ (DAIWA)
	a25-3009-01-03	CRYSTAL 32.768KHZ (DAIWA)
XTAL1	25-3045-01-00	CRYSTAL 3.6864MHZ (SUNNY)
	a25-3045-00-00	CRYSTAL 3.6864MHZ (DAIWA)
L42	25-1022-01-00	CHOKE COIL 1mH, +/-5% (TDK)
	a25-1022-00-00	CHOKE COIL 1mH, +/-10% (TDK)
R7-R10,R17	23-0013-10-02	RESISTOR 1K OHM +/-5% 1/4W
	v23-0013-10-00	RESISTOR 1K OHM +/-5% 1/4W
R19-R22	23-0151-10-02	RESISTOR 150 OHM +/-5% 1/4W
	v23-0151-10-00	RESISTOR 150 OHM +/-5% 1/4W
R13-R15	23-0333-10-02	RESISTOR 33K OHM +/-5% 1/4W
	v23-0333-10-00	RESISTOR 33K OHM +/-5% 1/4W

R5,R6,R18,	23-0472-10-02	RESISTOR 4K7 OHM +/-5% 1/4W
R16,R11,R12,	v23-0472-10-00	RESISTOR 4K7 OHM +/-5% 1/4W
R23-R25		
R1-R4	23-0222-10-02	RESISTOR 2K2 OHM +/-5% 1/4W
	v23-0222-10-00	RESISTOR 2K2 OHM +/-5% 1/4W
	a23-0222-16-00	RESISTOR 2K2 OHM +/-5% 1/16W
	a23-0222-16-01	RESISTOR 2K2 OHM +/-5% 1/16W
C30-C32,C63,	22-1100-21-03	ELEC CAP 10UF 16V +/-20%
C79,C80,C83	v22-1100-21-00	ELEC CAP 10UF +/-20% 16V
C38	22-3103-28-00	CER CAP 0.01UF +80 -20% 50V
	v22-3103-28-02	CER CAP 0.01UF +80 -20% 50V
	v22-3103-28-15	CER CAP 0.01UF +80 -20% 50V
C33-C37,	22-3104-28-33	MONO CAP 0.1UF +80 -20% 50V
C52,C59,	v22-3104-28-37	MONO CAP 0.1UF +80 -20% 50V
C65-C70,	v22-3104-28-40	MONO CAP 0.1UF +80 -20% 50V
C85-C91,	v22-3104-28-53	MONO CAP 0.1UF +80 -20% 50V
C81,C82	v22-3104-28-67	MONO CAP 0.1UF +80 -20% 50V
	v22-3104-28-68	MONO CAP 0.1UF +80 -20% 50V
C64,C39-C42	22-3470-26-00	CER CAP 47PF +/-10% 50V
C62	22-3221-26-00	CER CAP 220PF +/-10% 50V
C61	22-3271-26-00	CER CAP 270PF +/-10% 50V
C60	22-3331-26-00	CER CAP 330PF +/-10% 50V
C5-C12	22-3222-28-00	CER CAP 0.0022UF -20% 50V
C26-C29	22-6103-26-01	MYLAR CAP 0.01UF +/-10% 50V
	v22-6103-26-11	MYLAR CAP 0.01UF +/-10% 50V
	a22-6103-46-40	MYLAR CAP 0.01UF +/10% 100V
VC1	22-7002-01-00	TRIMMER CAP 20PF
	a22-7002-00-00	TRIMMER CAP 20PF
D1-D3	21-0001-00-00	DIODE IN4148 (FAIRCHILD)
	a21-0008-00-00	DIODE IN914 (FAIRCHILD)
	a21-0001-00-01	DIODE IN4148 (NEC)
	a21-0001-00-02	DIODE IN4148 (PHILIPS)
	a21-0001-00-03	DIODE IN4148
Q2	20-0025-03-00	TRANSISTOR 1402D (PHILIPS)
	a20-0041-00-01	TRANSISTOR 2N3904 (FAIRCHILD)
	a20-0041-00-00	TRANSISTOR 2N3904 (MOTOROLA)
	v20-0025-03-01	TRANSISTOR ST 1402D (SIEMENS)
	v20-0025-03-02	TRANSISTOR 1402D (PHILIPS)
Q1	20-0039-00-02	TRANSISTOR 2N3906 (FAIRCHILD)
	v20-0039-00-01	TRANSISTOR 2N3906 (MOTOROLA)

IBM® PC, PC/XT are registered trademarks of International Business Machines Corp.

uPD765 is a product of NEC Electronics Inc.

Z765A data sheets courtesy of Zilog Inc.

INS8250 data sheets courtesy of National Semiconductor Corp.

MSM6242 data sheets courtesy of OKI Electric Industry Co. Ltd.

R55C15 data sheets courtesy of RICOH Company Ltd.